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JANUARY 2016

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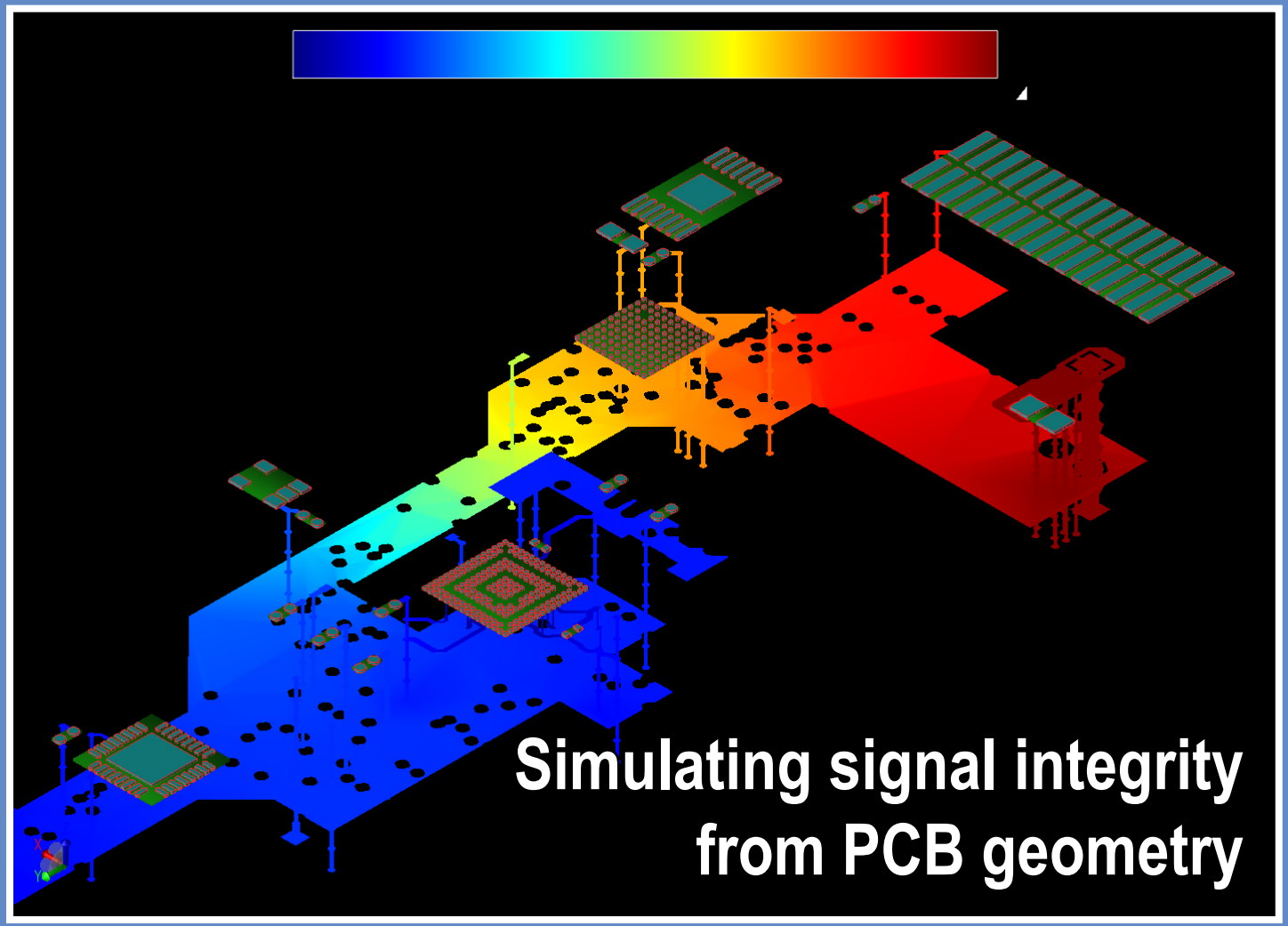

Simulating signal integrity from PCB geometry

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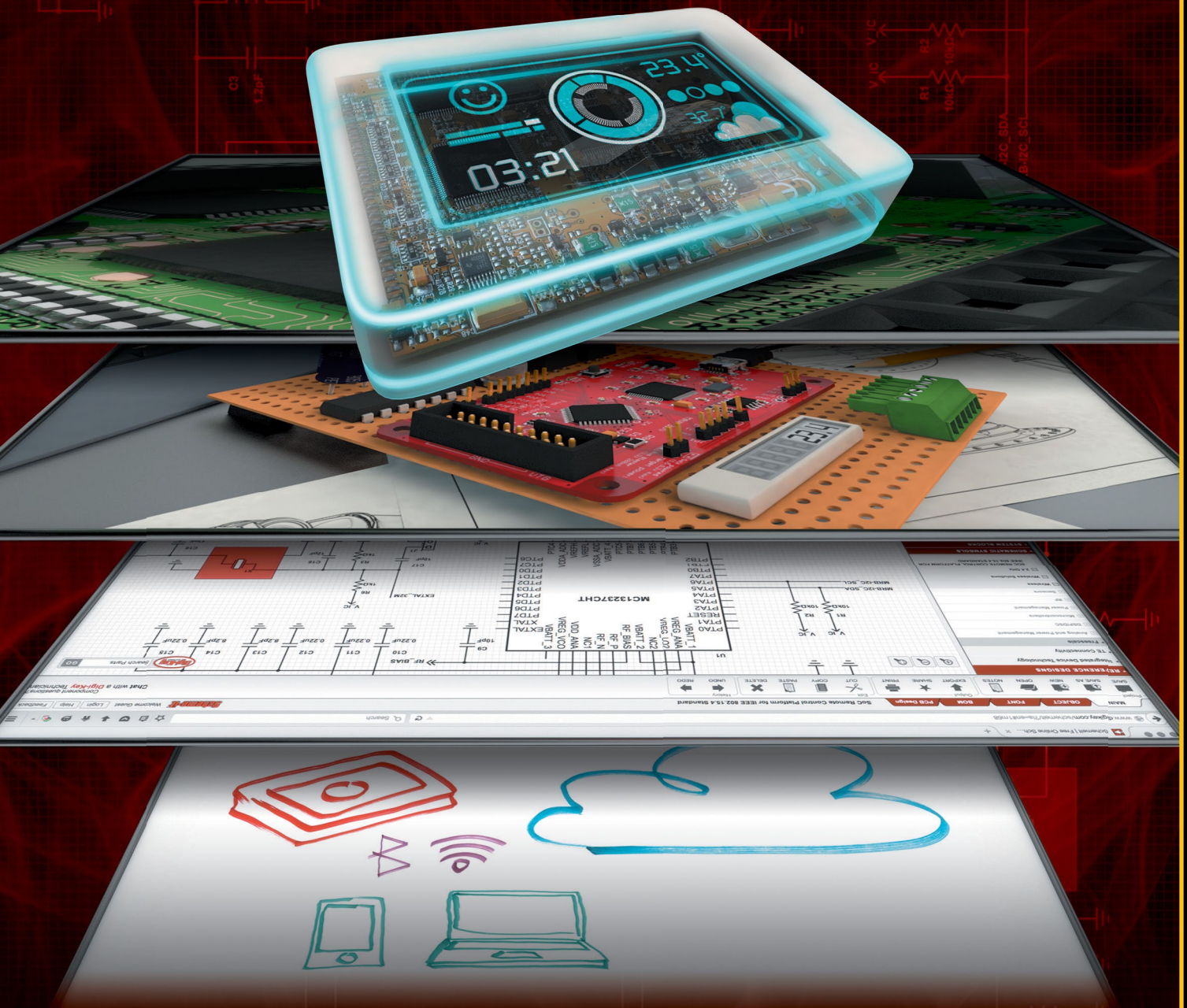

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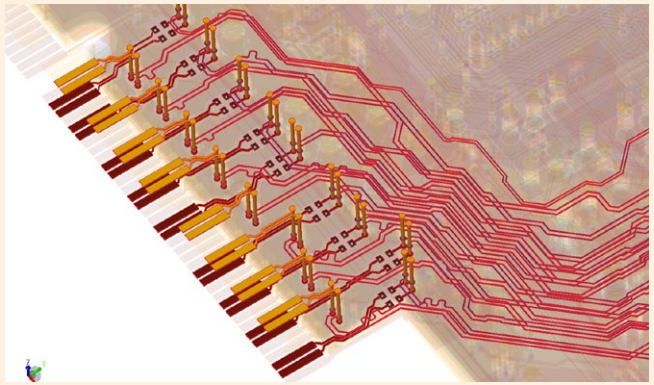


Keysight extends signal integrity/ power tools in ADS simulator

Keysight Technologies has added two electromagnetic (EM) software solutions designed to help signal integrity (SI) and power integrity (PI) engineers improve high-speed link performance in printed circuit board (PCB) designs. The solutions – SIPro and PIPro – will be available in the newest release of Keysight EEsof EDA's Advanced Design System (ADS) software. The ADS EDA software provides added capability in channel simulation technology for analysis of high-speed serial links and memory systems; it includes innovative EM-technology (electromagnetic) within a cohesive workflow for SI and PI design tasks, while the SIPro solution provides speed and accuracy for EM characterisation of high-speed links on densely-routed, highly complex printed circuit boards. There are three new simulation engines for power integrity. More information in the longer item here.

FEATUREARTICLES

ONLINE THIS MONTH

Mobile device proximity sensor manages RF exposure while maintaining network connectivity
by David Wong, Semtech

Review: Rohde & Schwarz FPH spectrum analyser
by Kenneth Wyatt, EDN

How to suppress interference on LVDS connections
a paper from Langer EMV-Technik

EDN's columns

4 REASONS FITBIT IS BEING SUED FOR INACCURATE HEART-RATE MONITORS

This month, I am turning this column over to US EDN's Patrick Mannion; it is never comfortable when legal disputes invade "our" engineering domain, and Patrick has some very salient points relating to this episode. The following is an edited version of Patrick's column: you can read his original, which includes commentary specific to the US legal context, here - GP.

There are at least four reasons Fitbit was just hit with a class-action lawsuit over the inaccuracy of its $150 Charge HR and $250 Surge heart-rate monitors. Oddly, it has almost nothing to do with engineering, design, or software. The first two have to do with questionable tort laws, and consumer and lawyer greed (combined with a little anger). Third is tied to a bad marketing mistake by Fitbit, while the fourth is more interesting, having to do with the difficulty of accurate heart-rate (HR) monitoring on a consistent basis. Mismanaged expectations and poor customer service are more to blame than engineering and software.

[There is a point] in that while many plaintiffs have legitimate gripes, whatever happened to "buyer beware"? Few companies set out to deliberately deceive their customers. Is it really necessary to go after them legally if a product didn't behave as you thought it should? If it's a serious medical device, sure. But a fitness gadget? Seriously? I'm very keen to see the outcome of this case as it could greatly impact innovation, as well as how devices are marketed.

Which brings us to point three: Fitbit's marketing mistake.

Consumers don't like to feel deceived. A company usually gets one chance to make it right: when the customer calls to complain. In this case, Fitbit blew it on both levels. When the users called to gripe about the HR accuracy, they should have accepted the complaint, also known as "free customer survey response" and offered a refund.

Instead, Fitbit chose to stand behind their product, the engineering of which was completely undermined by an awful marketing mistake: they should never have said "every beat counts." Once that statement got out, even if Fitbit isn't claiming to be able to measure every beat, the consumers are led to the assumption that the device can measure every heart beat, and anything short of that is a "bad" product. Oops!

That simple tagline, combined with poor customer service, opened the door to a class action lawsuit that may well be settled before it ever gets to court, but the damage is done. This is one reason it's hard to be an engineer. Not because the job is hard, that's a given, but because really good work can easily get undermined by something as inane as a marketing tagline.

Let's assume, then, that the engineers were really trying to get the best HR monitor possible out to market. So why did it seem to fall so short on accuracy? Note that the plaintiffs in the case aren't alone: reviewers also noted its wayward ways.

Companies have been doing accurate HR monitoring for many years using sensors on a chest strap. Serious athletes don't mind the hassle. Casual exercisers are a different story: it's awkward and uncomfortable, so wrist-based monitoring is the technique of choice for Fitbit, and for many other consumer HR monitoring OEMs, including Apple for its watch.

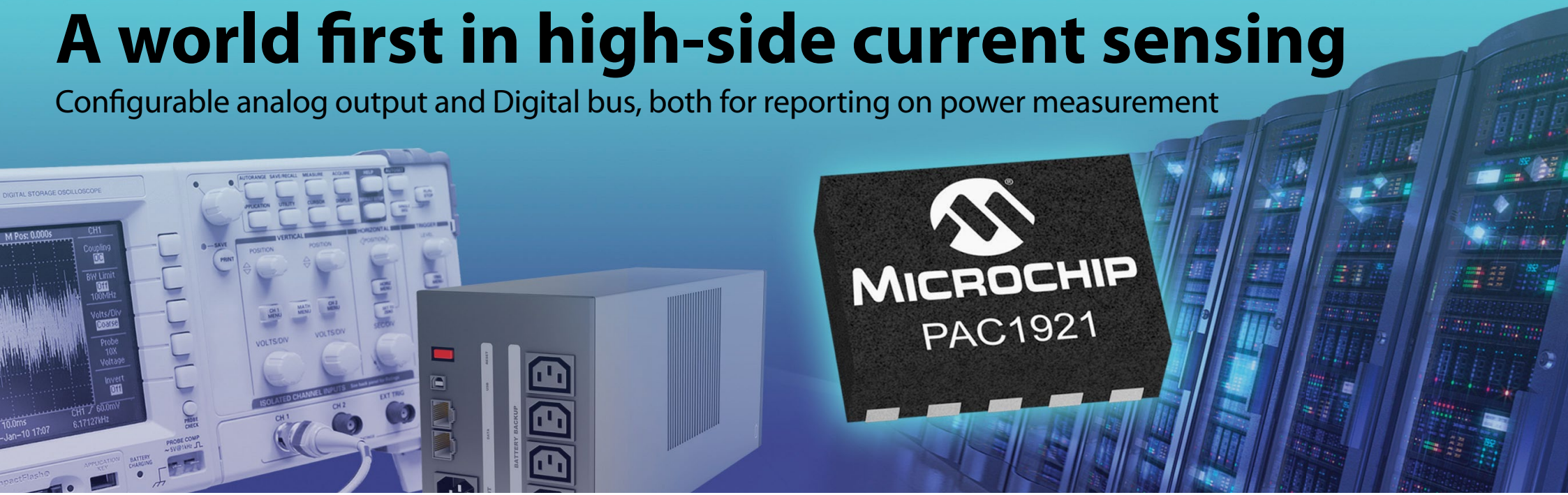
But we've been doing this for some time already, so why the inaccuracy in HR monitoring? Fitbit was using photoplethysmography (PPG). This technique measures light absorption through blood and correlates that with the heartbeat as blood volume increases and decreases. Green light (530 nm) is typically used, as that wavelength has been shown to give the most accurate results when compared to an electrocardiogram (ECG), the gold standard.

While PPG is good in a steady state, it's at the end of the arm, and is therefore in constant motion, the more so during exercise. This causes large variations in blood volume due to centrifugal force, so it becomes increasingly difficult to separate out high volume in a blood vessel due to systolic pressure versus centrifugal force acting on the blood. [MEMS accelerometers can be, and are, applied to derive a measure of motion to allow compensation]. This variation is compounded by other variables, such as ambient light, which must be measured and [also] compensated out, causing measurement delays as readings settle.

For now, PPG isn't perfect, but highly motivated engineers and software developers are "on the case" so it will improve. In the meantime, let's not let marketing get ahead of us again. Gotta manage those expectations a bit more carefully: and consumers need to remember *caveat emptor.*

A world first in high-side current sensing

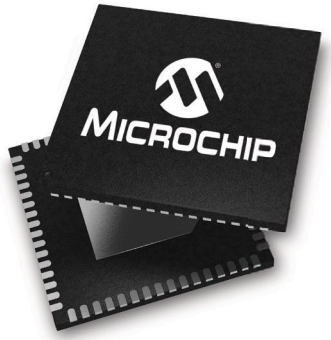
Configurable analog output and Digital bus, both for reporting on power measurement



Microchip's PAC1921 is the world's first high-side current/power sensor to present power, current or voltage over a single output pin.

Using the 2-Wire digital bus to maximise data and diagnostic reporting, and the configurable analog output to minimise data latency, the PAC1921 increases flexibility in high-speed power management applications.

The PAC1921's analog output can be adjusted for 3V, 2V, 1.5V or 1V microcontroller inputs and measure system-load power from 0V to 32V.



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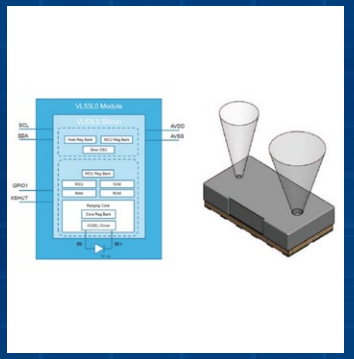
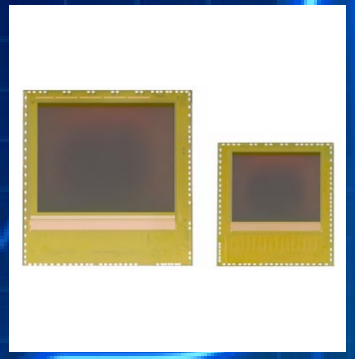



Melexis
MLX92292

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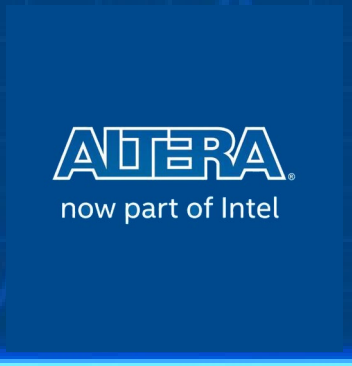
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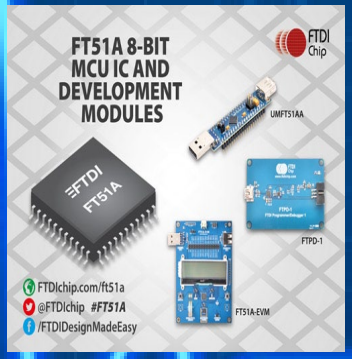
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Highest-performing audio op amp, claims TI

Citing lowest distortion and noise, high linear output current, and low power, Texas Instruments says its latest audio amplifier pushes the boundaries for professional and portable audio. The OPA1622 is an addition to the company's Burr-Brown Audio line and is the next generation of the OPA1612. The OPA1622 delivers high output power of up to 150 mW and extremely low distortion of -135 dB at 10 mW into a 32-Ω load, enabling the highest performance for professional audio equipment. The OPA1622's small size, low power consumption and low distortion can deliver high-fidelity audio in portable devices such as headphone amplifiers, smartphones, tablets and USB audio digital-to-analogue converters (DACs). The OPA1622 op amp is optimised for high-fidelity portable audio devices: it consumes quiescent current of 2.6 mA per channel and delivers high linear output current of 80 mA rms in a 3 x 3-mm dual flat no-lead (DFN) package. Increased power-supply rejection ratio (PSRR) of -97/-123 dB at 20 kHz enables low distortion from switching power supplies with no low-dropout regulator (LDO), saving board space without compromising audio performance. The device costs $2.90 (1000).

A TINA-TI SPICE macromodel is available for the OPA1622 to help designers verify board-level signal-integrity requirements. A TI Designs – Precision reference design for voltage-output audio DACs will be available in 1Q16 for OPA1622-based headphone amplifier designs.

Complete article, here

Mouser/NI board design software ramps up power with $300 version

Mouser Electronics has posted details of a new variant of its circuit- and PCB-design software; positioned at a low-cost point, Mouser says that the package is capable of taking many small-medium (and upwards) designs to completion, offering advanced design support.

Mouser is a reseller of NI's MultiSIM Full Edition; the standard NI circuit design environment that includes schematic capture integrated with comprehensive simulation tools. At the other end of the scale the distributor has been offering a free download of MultiSIM Blue – to give it its full title, "NI Multisim Component Evaluator Mouser Edition". This is a circuit simulation

package that integrates printed-board design and bill-of-materials features; it allows the user to carry out schematic capture, to simulate, do PCB layout, BOM and purchase all in one integrated tool. Although has limitations (but not in board size, and it does allow up to 64 layers, with autorouting) Mouser claims that, “no other free tool gives you this level of integration... an easy-to-use, seamless environment for the functional simulation of linear circuits using the Berkeley SPICE Engine along with advanced electronic components.”

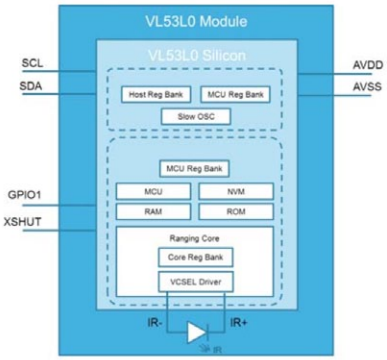
Now, however, Mouser has introduced an intermediate version that is not free, but offers – the distributor says – a great deal of design power for a modest cost. MultiSIM Blue Premium uses a subscription model; $299 per year. It has no limitations on number of components per board and Mouser says it represents two or three times [the capability] of what has been available at this level. The integration is retained, tagged as “four circuit design tools in one”, a professional integrated circuit design tool. Unlimited components and unlimited custom components are now available in this Premium edition, along with unlimited schematic sheets, and forward and back annotation. Hierarchical design capability is available with unlimited levels. Over 16,000 additional parts are included from the National Instruments Master database.

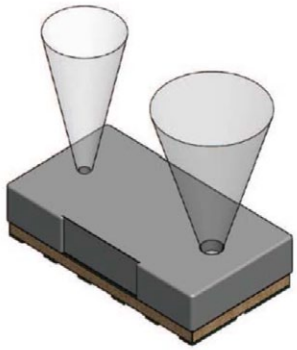
Complete article, here

Time-of-flight ranging sensor for cameras, robotics, IoT

Promising to ‘revolutionise mobile-camera performance and enable new applications in robotics and IoT', ST Microelectronics’ FlightSense VL53L0 low-power, miniature sensors can be used for fast autofocus in smartphones, for proximity sensing, and object detection.

This is ST’s second-generation laser-ranging sensor based on its FlightSense technology. VL53L0, can range faster, over longer distances, and more accurately. In a form factor of 4.4 x 2.4 x 1 mm, ST says the VL53L0 is the smallest ToF (Time-of-Flight) module available, and the first to integrate a 940 nm VCSEL (vertical cavity surface-emitting laser) light source, a SPAD (single-photon avalanche diode) photon detector, and an advanced microcontroller to manage the complete ranging function. Being the market’s first module to use light emitted at 940 nm, coupled to leading-edge infrared filters, the VL53L0 maximises ambient light immunity and is now invisible to the human eye. The embedded microcontroller and digital algorithms minimise both the host processing and system power consumption in the final application. The VL53L0 is able to perform a full measurement operation in one image frame, typically less than 30 msec, at distances beyond 2m. With such performance levels the camera system can achieve instant focus in both video and burst modes, even in low-light or low-contrast scenes, which are especially challenging. VL53L0 also enhances smartphone applications including dual-camera-based depth-mapping and offers opportunities in robotics, user detection, drones, IoT, and wearables.





Complete article, here

Portable 500 MHz scope has bench-scope performance

Rohde & Schwarz' Scope Rider instrument is presented as the first handheld oscilloscope with the functionality, and touch and feel, of a comparable lab oscilloscope. The company says that it has taken a completely fresh look a the requirements of this section of the scope market; R&S contends that the feature set offered by the major manufacturers in the hand-held/portable scope area have changed little since the introduction of Fluke's ScopeMeter, in the (literally) last century. Although there are several portable scope formats on offer – some from smaller players in the T& M arena – the company says most are very limited in matters such as acquisition rate, image quality and screen area. It follows recent bench scope trends in being touch-screen operated. R&S designed the "RTH" as a general purpose instrument for field use, but with specific features of use to the power test area, such as testing electrical machines, inverters and drives, and photovoltaic installations.

Accordingly, the instrument is battery powered (not grounded) and has (opto) isolation between each of its input channels, and its logic board, and the communications interfaces. The isolation is rated for work on industrial systems. It can also be operated remotely via Ethernet connection, so that it can be connected to a unit under test, and the operator can withdraw to a safe distance before commencing live testing.

It has an acquisition rate of 50,000 waveforms per second, a 10-bit A/D converter developed by Rohde & Schwarz and a maximum bandwidth of 500 MHz for the analogue input channels. Base specifications can be upgraded (in bandwidth) by software key.

The unit integrates five functions, around a high-performance oscilloscope featuring a precise digital trigger system, 33 automatic measurement functions, mask test and XY diagram mode. It can function as a logic analyser with eight additional digital channels (an extra module is required), as a protocol analyser with trigger and decoding capability, as a data logger and a digital multimeter. The scope has a low noise floor, and derives 9-bit resolution from a 10-bit A/D converter. It includes preset and adjustable filtering, in both analogue and digital paths. The 4-channel variant has a voltmeter function: in 2-channel form, the extra internal space houses a full DVM feature set. The unit's price range is (very approximately) €2700/£2000 to around double that, the entry point being a 2-channel instrument with 60 MHz b/w and DMM. The high-end, 500 MHz bandwidth option is "unique" in this sector, R&S says. More information via the link below.

There will be an option to carry out FFT-based spectrum analysis on the instrument; meanwhile, late last year, R&S introduced its FPH hand-held spectrum analyser in the same physical format – you can read EDN's review of that unit, in a article here.

Complete article, here

No-code, no-static-power state machine in mixed-signal programmables

Silego Technology's fifth generation of its GreenPAK (GPAK) programmable mixed-signal ICs, the SLG46531V GPAK 5, joins the company's configurable mixed-signal ICs (CMICs), adding functions such as an asynchronous state machine, and I²C for on-the-fly reconfiguration. This latest generation device, including Silego's new Asynchronous State Machine and I²C blocks, adds flexibility, functionality, and ease of design to the NVM programmable GPAK family of devices. With the addition of the asynchronous state machine, designers can implement up to eight unique states with zero code, zero static power, and fail-safe operation. The addition of I²C enables designers to change device configuration, such as analogue comparator thresholds, on-the-fly. The I²C block can also act as a digital IO expander. Included in the SLG46531V are improved counter/delay blocks, featuring one-shot and frequency detect modes, as well as the capability to drive an external crystal oscillator. These new functions, along with the configurable digital and analogue blocks seen in previous generations of GPAK, are all packed into a 2.0 x 3.0 mm 20-pin STQFN with 18-GPIO.

Complete article, here

Magnetic latch/switch family with ASIL B rating

Programmable micropower devices are positioned as the first in the industry to offer ASIL B automotive functional safety;

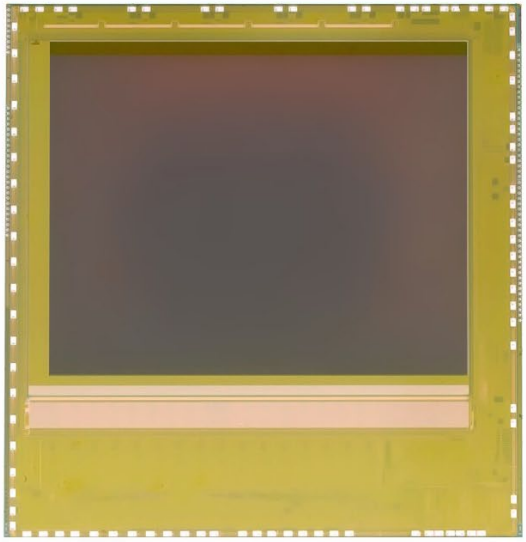
Melexis (Tessenderlo, Belgium) has introduced a magnetic sensing technology for automotive design. MLX92292 represents, the company asserts, a new way of sensing. This device delivers switch and latch functions, but unlike existing products on the market it can determine the presence of magnetic fields that are lateral, not just orthogonal, to it. The uniqueness of this offering is taken further by the fact that the MLX92292 latch/switch is the only one to currently support ASIL B safety integrity level (in accordance with ISO 26262), with an array of built-in diagnostic mechanisms available. Flexibility is a key attribute of the MLX92292; users can choose straightforward pre-programmed units, or end-of-line (EoL) program-

ming capacity. Through this each device may be configured (via its output pin) during the OEM production process. The programming facility also enables setting of both magnetic operating points to small increments across a range spanning -90 mT to +90 mT. Housed in 3-lead TSOT or TO92 package formats, with an operating voltage range from 3.3V to 18V, the MLX92292's low power consumption (typically drawing 7 µA) makes it suitable for battery-powered operation. As sleep time is a programmable parameter, power consumption can be matched with specific power budget needs. Target applications include brake lights, steering sensors and handbrake mechanisms.

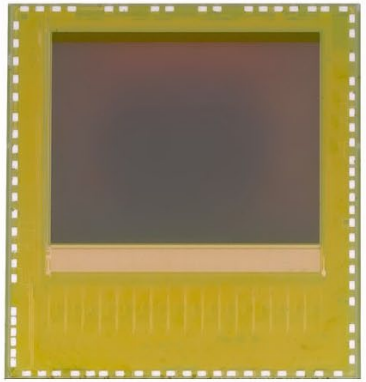
Complete article, here

3D image sensor chips put VR on smartphones

Infineon Technologies and pmdtechnologies have disclosed their REAL3, 3D image sensor chips that will allow mobile devices to quickly and realistically detect their surroundings in three dimensions. Image sensor chip applications include the spatial measurement of rooms and objects, indoor navigation and the implementation of special photo effects: however, the immediate application is to enable “extremely realistic virtual and augmented reality game experiences” that involve the interaction of the gamer’s own hands and his living environment within the game, via head-mounted devices.
Compared to the previous version, the optical sensitivity as well as the power consumption of the new 3D image sensors has been improved, Infineon says. With built-in electronics that take up little space, the chips make it possible for cell phones to operate mini-camera systems that can measure 3D depth data.



Using microlenses for high sensitivity, the camera’s range and measurement accuracy depend on two factors: on the intensity of the emitted and reflected infrared light, and to a significant extent on the pixel sensitivity of the 3D image sensor chip. The optical pixel sensitivity of the new 3D image sensor chips are now double that of the previous version. The improved optical pixel sensitivity is the result of applying one microlens to each of the pixels of the 3D image sensor chip.



The 3D image sensor chips showcased at the (January 2016) Consumer Electronics Show were specifically designed for mobile devices, where most applications only need a resolution of 38,000 pixels. The previous 100,000-pixel matrix was accordingly scaled down, and other functional blocks, such as the analogue/digital converter, have been optimised for chip area and performance range. System costs are lower: the sensor chip area is almost halved, and, because of the lower resolution, smaller and less expensive optical lenses can be used.

Complete article, here

ZigBee/EnOcean cooperation for energy harvesting on ZigBee 3.0

The ZigBee Alliance and the EnOcean Alliance are to cooperate on combining the benefits of EnOcean energy harvesting wireless solutions with ZigBee 3.0. The two organisations say that joint development of an open, global specification for energy harvesting wireless communication technology will help meet growing demand for interoperable, self-powered IoT sensor solutions.

A new specification will take advantage of both alliances' expertise and standards-development processes in furthering energy harvesting device interoperability: it will bring together the EnOcean Equipment profiles (EEPs) for sub-GHz networking with the recently-ratified ZigBee 3.0 solution in the 2.4 GHz frequency band.

A Technical Task Force will be built of ZigBee Alliance and EnOcean Alliance representatives to define the technical specifications required to combine standardised EnOcean Equipment Profiles (EEPs) with the ZigBee 3.0 solution, which operates in the worldwide IEEE 802.15.4 2.4 GHz standard. The alliances plan to complete definition of this technical specification and share details of associated collaborative marketing and business activities in the second quarter of 2016.

Complete article, here

Multifunction scope provides sync'd multi-domain signal views

Tektronix' MDO4000C Series of Mixed Domain Oscilloscopes can be configured with up to six instruments in a single unit including a full spectrum analyser. The MDO4000C provides a synchronised view of analogue and digital waveforms along with RF spectrum traces, for use as a debug tool for Internet of Things (IoT) and other embedded engineering applications. Like the 6-in-1 MDO3000, the MDO4000C expands on its core oscilloscope functionality with options to add a spectrum analyser, arbitrary/function generator, logic analyser and protocol analyser. A digital voltmeter (DVM) is free with product registration.

As an oscilloscope, the MDO4000C features long record length, fast sample rate and fast waveform capture rate to help uncover elusive problems. Performance enhancements compared to the MDO3000 integrated oscilloscope include: 20 Mpoint record length, up to 5 Gsample/sec on all channels, >340,000 waveforms/sec capture rate and a 50% larger display; up to 6 GHz spectrum analyser with better spectrum analyser performance, the ability to synchronise views across time and frequency domains, and the ability to perform vector signal analysis; logic analyser timing resolution down to 60.6 psec and independent logic thresholds per channel enabling capture of multiple logic families at once; and protocol analysis for up to three buses simultaneously with triggering up to 500 Mb/sec.

The MDO4000C can be configured as a base oscilloscope with an entry price of $7,300. A 3- or 6-GHz spectrum analyser, arbitrary/function generator, 16 logic channels, or protocol support can be added at the time of purchase, or added later as an upgrade, allowing it to precisely conform to every lab's needs and budget. Oscilloscope bandwidth extends from 200 MHz to 1 GHz and can also be upgraded.

Complete article, here

LoRa programme boosted by Semtech/ST collaboration

Programme to scale LoRa technology to meet high-volume demands of Internet of Things applications; ST has announced it will offer a product line including LoRa systems on chips (SOCs) to accelerate deployments of low-power wide-area networks by mobile network operators (MNOs). The two companies have set up an agreement around Semtech's LoRa long-range wireless RF technology. ST intends to use the technology to target Internet of Things (IoT) deployments by mobile network operators (MNOs) and large-scale private networks.

ST will join the LoRa Alliance and release reference designs for LoRa technology based on its STM32 family of microcontrollers. ST plans to develop microcontrollers with on-chip LoRa technology that supports the LoRaWAN standardised protocol. Semtech and ST will cooperate to integrate LoRa technology into multiple platforms that target a variety of applications for several business initiatives around LoRa.

ST joins the LoRa Alliance, with its LoRa ecosystem, with the intention of helping standardise LoRa and LoRaWAN for IoT low-power wide-area networks (LPWAN) worldwide. Both Semtech and ST believe standardisation and a strong ecosystem will foster technology adoption to achieve the large volumes projected for IoT.

Complete article, here

Hybrid supercap completes UL certification, aims to replace Li batteries

by Paul Buckley

The developer of an innovative supercapacitor-based energy storage and battery enhancement technology, Paper Battery Company, has completed UL certification for the company's PowerResponder product range. PowerResponder is a range of hybrid supercapacitors with technology enhancements that, its designers hope, may replace traditional lithium ion batteries in select applications. PowerResponder has also been certified as RoHS compliant, giving it added environmental and safety benefits. The product line will be available in a range of sizes from 90F to 9000F with initial products available to OEM customers by the end of the year.

The company comments, "By rapidly recharging - or energy-snacking as we like to call it - customers can now carry just the amount of energy needed for their tasks, with high availability of their device due to the turbo-charging in seconds not hours. The long cycle life of PowerResponder makes it possible to integrate the cell as part of the product, with a life as long as, or longer than, the product it powers."

Compared to a typical lithium ion battery, PowerResponder claims to provide 10X higher peak pulse power capacity, 100X greater cycle life, higher reliability in high temperature applications, lower energy density, holds charge with a similar low leakage current and is much safer with no risk of flammability or explosion with runaway heating.

Complete article, here

Intel finalises Altera acquisition

Intel has announced that it has completed the acquisition of Altera, re-stating its position that the acquisition, "complements Intel's leading-edge product portfolio and enables new classes of products in the high-growth data center and Internet of Things (IoT) market segments."
Altera will operate as a new Intel business unit called the Programmable Solutions Group (PSG), led by Altera veteran Dan McNamara. Intel says it, "is committed to a smooth transition for Altera customers and will continue the support and future product development of Altera's many products, including FPGA, ARM-based SoC and power products. In addition to strengthening the existing FPGA business, PSG will work closely with Intel's Data Center Group and IoT Group to deliver the next generation of highly customised, integrated products and solutions.

"...together we will make the next generation of semiconductors not only better but able to do more," said Brian Krzanich, Intel CEO. "We will apply Moore's Law to grow today's FPGA business, and we'll invent new products..."

Complete article, here

GreenPeak bundle aims to step up the 'smart' in smart-home

Founder and CEO of the low power RF semiconductor company for Smart Home and IoT connectivity GreenPeak – Cees Links – has for some time been a vocal proponent of the position that our efforts to add connectivity and make our houses "smart" have been severely lacking in the "smart" dimension.
Accordingly, GreenPeak is presenting its Family@Home Solution to "transform the Smart House into a Smart Home... the first application that combines the best of Family Lifestyle monitoring with Smart Home services that provides peace of mind for busy families."
The Family@Home application is based on a self-learning algorithm with behaviour pattern recognition. No rule-based programming is required and exceptions are automatically reported. Family@Home provides intelligent status updates in a dashboard app and generates alerts when something unexpected happens at home or with family members.
This new smart service combines sensors for monitoring family activities with a variety of automated home applications such as temperature and climate control, home monitoring, lighting systems, appliance control, intruder detection, etc. "The tech industry has been telling consumers that they need a Smart Home but, up until now, all they are being offered are connected devices – creating a 'house with sensors', says Cees Links, CEO and Founder of GreenPeak Technologies. "Consumers don't want connected things – they want smart applications that take care of their family and their home. That is why GreenPeak is working with the world's leading service providers to transform a "house with sensors" into the "Smart Home".

Complete article, here

Multi-sensor development kit to accelerate IoT product programmes

To save time in developing Internet of Things (IoT) projects, quickly creating a demo or proof of concept is key, says Bosch, introducing its XDK, or Cross Domain Development Kit, a rapid prototyping tool that enables developers to quickly bring their IoT designs to life.

XDK is a fully integrated hardware and software product, including a MEMS accelerometer, magnetometer and gyroscope, as well as humidity, pressure, temperature, acoustic and digital light sensors. The kit includes Bluetooth and WiFi connectivity, a microcontroller, integrated antennas, a micro SD card slot and a rechargeable battery.

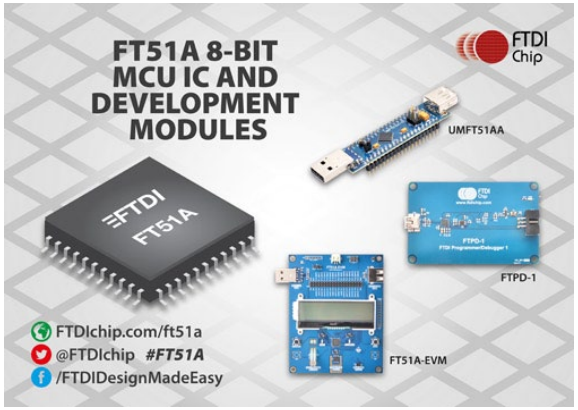
The software development environment offers access to different API layers which allow the user to program at their preferred depth. An algorithm library and sample applications are provided, as well as access to an online community to share information and support projects. The XDK was designed to allow users an easy transition from prototype to mass production by providing a clear road to product development.

Complete article, here

FTDI adds board-level products around its 8051-based micro core

Creating an 'ecosystem' to accompany its 8-bit FT51A MCU, FTDI Chip has designed a series of modules that exploit the features available on its connectivity-oriented, 8051-compatible device.

The processing core of the FT51A MCU executes an 8051 feature set (capable of running at 48 MHz). Along with this, it possesses a wide array of interfaces - including USB client, UART, SPI, I²C, 245 FIFO, PWM and GPIO options. The USB hub feature, which is completely unique to this IC, allows multiple USB-enabled devices to be cascaded or combined with one another. The FT51A's data conversion capabilities comprise an 8-bit ADC. Its 16 kB shadow RAM accelerates read access of the core, thereby heightening throughput levels. Low power operation is another key characteristic of this device, drawing 20 mA (typical) while active and 150 µA (typical) when in suspend mode.



The FT51A-EVM evaluation module provides different functions to demonstrate the FT51A MCU's application parameters - in particular its suitability for multi-sensor circuits. In a 40-pin dual-in-line (DIP) package, the UMFT51AA also features an FT51A MCU. This compact module provides engineers with a drop-in replacement for legacy 8051 MCUs via a DIP socket.

The FTPD-1 is a credit card sized programmer/debugger module which accompanies the UMFT51AA and FT51A-EVM. Through its FT230X USB-to-UART conversion IC and dual buffer it can generate a single line half-duplex UART signal with no handshake.

Complete article, here

PAM4: A NEW MEASUREMENT SCIENCE

By Martin Rowe, EDN

As the world's insatiable appetite for data keeps growing, engineers must continuously develop new technologies to move bits ever faster. With 100 Gbps serial links in rapid deployment, engineers are under pressure to develop the next higher speed: 400 Gbps Ethernet and others are beginning to take shape. But, the shape of the waveforms looks to be quite different this time.

With previous speed increases, engineers have found ways to keep using the traditional NRZ (non-return-to zero) modulation where one baud carries one bit. But as individual links move from 25-28 Gbps to 50-56 Gbps, NRZ could be reaching its limit. That's because the bandwidth required to carry NRZ could just be too much to be cost effective. Plain old PCBs just can't handle it, making signal losses intolerable. NRZ just might be running out of steam. Of course, we've heard that before.

Enter PAM4; PAM4 should let you develop 56 Gbps data lanes with less signal loss than would occur by simply doubling the NRZ—sometimes called NRZ-PAM2—bit rate. Exotic PCB materials can compensate for the deficiencies, but at a cost few are willing to pay.

PAM4 doubles the bit rate for a given baud rate over NRZ. Thus, a 28 Gbaud PAM4 signal can deliver the same bit rate as a 56 Gbaud NRZ signal. Figure 1 shows the difference between NRZ (left) and PAM4 (right).

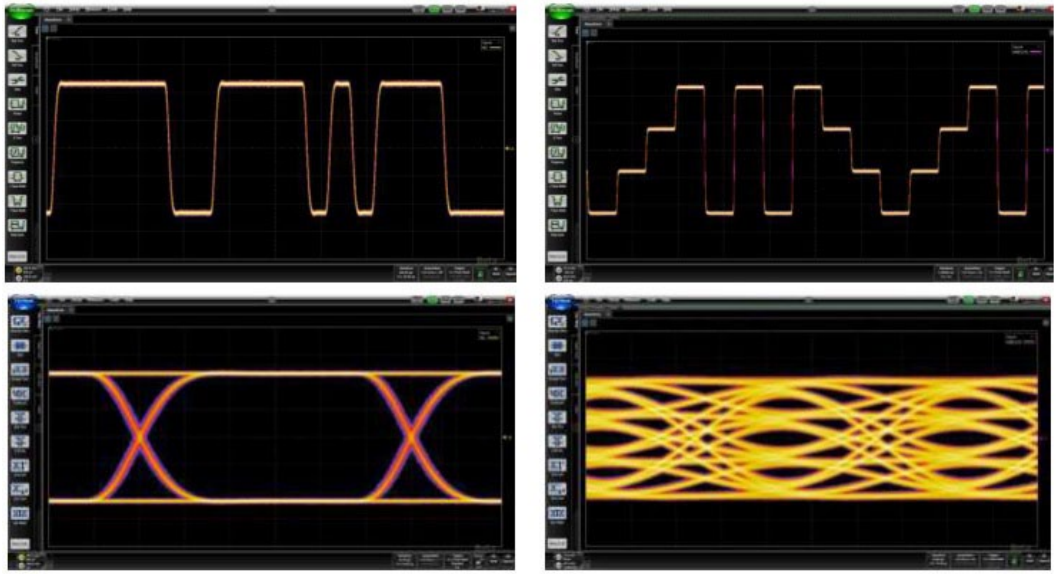


Figure 1. *An NRZ data stream (top left) uses two voltage levels and produces a single eye (bottom left). A PAM4 data stream (top right) uses four levels, producing three eyes (bottom right). (Image courtesy of Keysight Technologies)*

Besides the bandwidth advantage, PAM4 can result in the need for fewer PCB traces. At 56 Gbps, 400 Gbps Ethernet can be realised with four lanes of PAM4 but might require eight 28 Gbps lanes with NRZ. Thus, PAM4 can reduce the traces in half, reducing the risk of crosstalk and making a PCB designer's job easier.

There's more than one way to encode bits onto a PAM4 signal. Figure 2 shows one possible coding of bits; this one uses a Gray code. The goal of an encoding scheme is to minimise the number of bit transitions, which can improve signal integrity.

Lower bandwidth means less loss at a given frequency and fewer PCB circuit traces. That's the good news. The bad news is that PAM4 trades off bandwidth for SNR (signal-to-noise ratio). That makes PAM4 eyes more sensitive to noise than NRZ eyes. "Because it has three eyes, PAM4 divides SNR by three as compared to NRZ," noted Patrick Connally, Technical Marketing Engineer, High Bandwidth Oscilloscopes at Teledyne LeCroy. As a result, PAM4 receiv-

ers will need three slicers to detect the eyes, as Figure 3, from a DesignCon 2015 paper, shows. The additional slicers add complexity and cost to receivers.

There are other tradeoffs, too. Take a look at the simulated PAM4 signal in Figure 2. In the middle eye, the widest point is at half the eye's amplitude. But, that's not the same for the upper and lower eyes where the widest eye opening may occur at about the 1/3 or 2/3 point in the eye amplitude. The compression occurs because rise and fall times have finite speeds, cutting off parts of the eyes. The nonlinear eyes can result in DDJ (data-dependent jitter), a form of intersymbol interference.

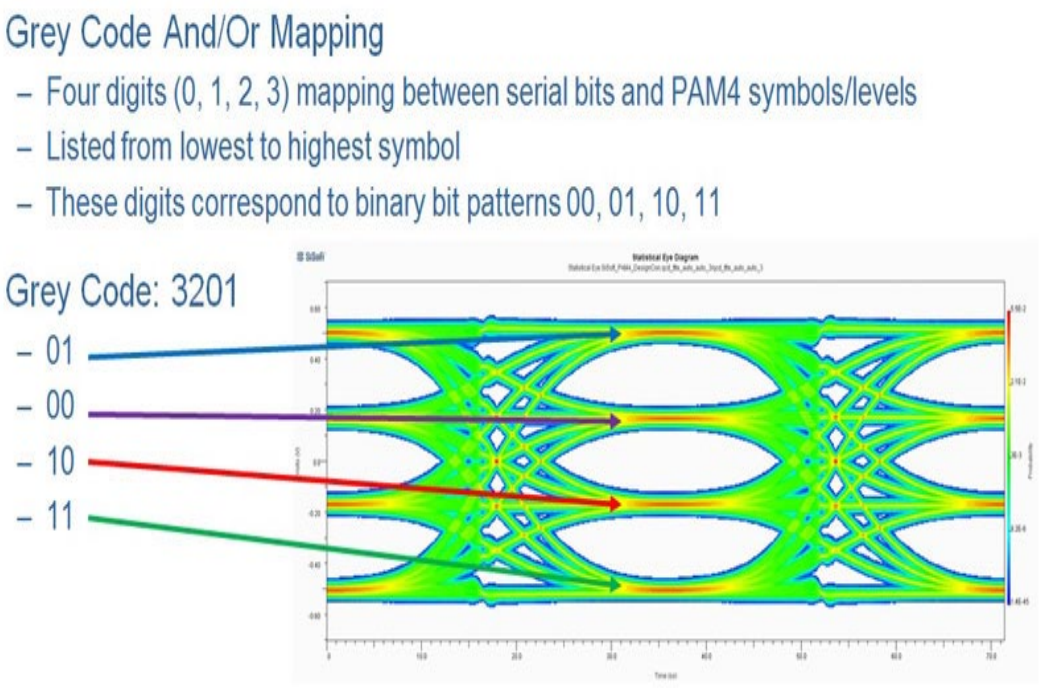


Figure 2. *This simulated PAM4 eye shows how the signal might be coded to get four levels and thus two bits per baud. (Image courtesy of SiSoft)*

Another issue with PAM is timing skew... *the article continues with further issues that will challenge test& measurement tools at these higher speeds, click for pdf.*

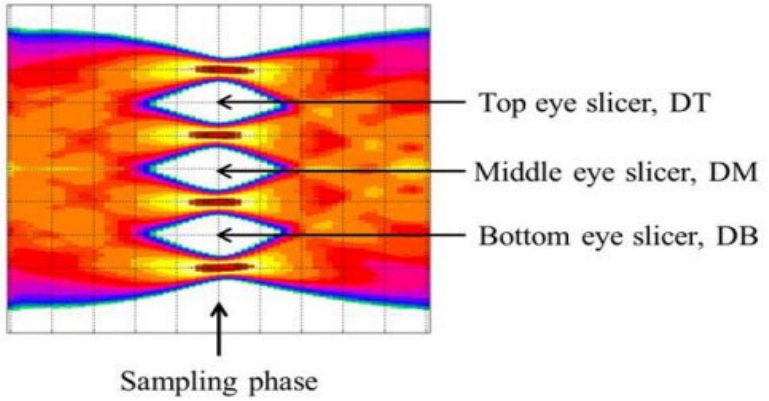


Figure 3. *A PAM4 receiver will need three slicers to detect the three eyes.*

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DIGITAL SIGNAL ANALYSIS WITH BANDWIDTH UP TO 500 MHZ

By Martin Schmähling, Rohde & Schwarz

Modern signal and spectrum analysers can demodulate and analyse not only pure spectrum measurements but also complex modulated signals for wireless communications systems. The analysis bandwidth represents the maximum signal bandwidth that can be demodulated and is therefore an important performance feature of these analysers.

A high analysis bandwidth is also beneficial for measurements on pulsed signals such as those from radar systems. The analysis bandwidth determines the resolution in the time domain, and therefore the minimum pulse length that can be displayed. Extending analysis bandwidths beyond what has routinely been available in the past – to 500 MHz – represents a new option that offers many advantages when characterising communications signals.

Communications modulation bandwidths trend upwards

The trend in digital communications is towards ever faster data rates, which require higher frequency bandwidths for transmission. In mobile communications the channel spacing for GSM was established at 200 kHz, whereas for UMTS it had expanded to 5 MHz. The cur-

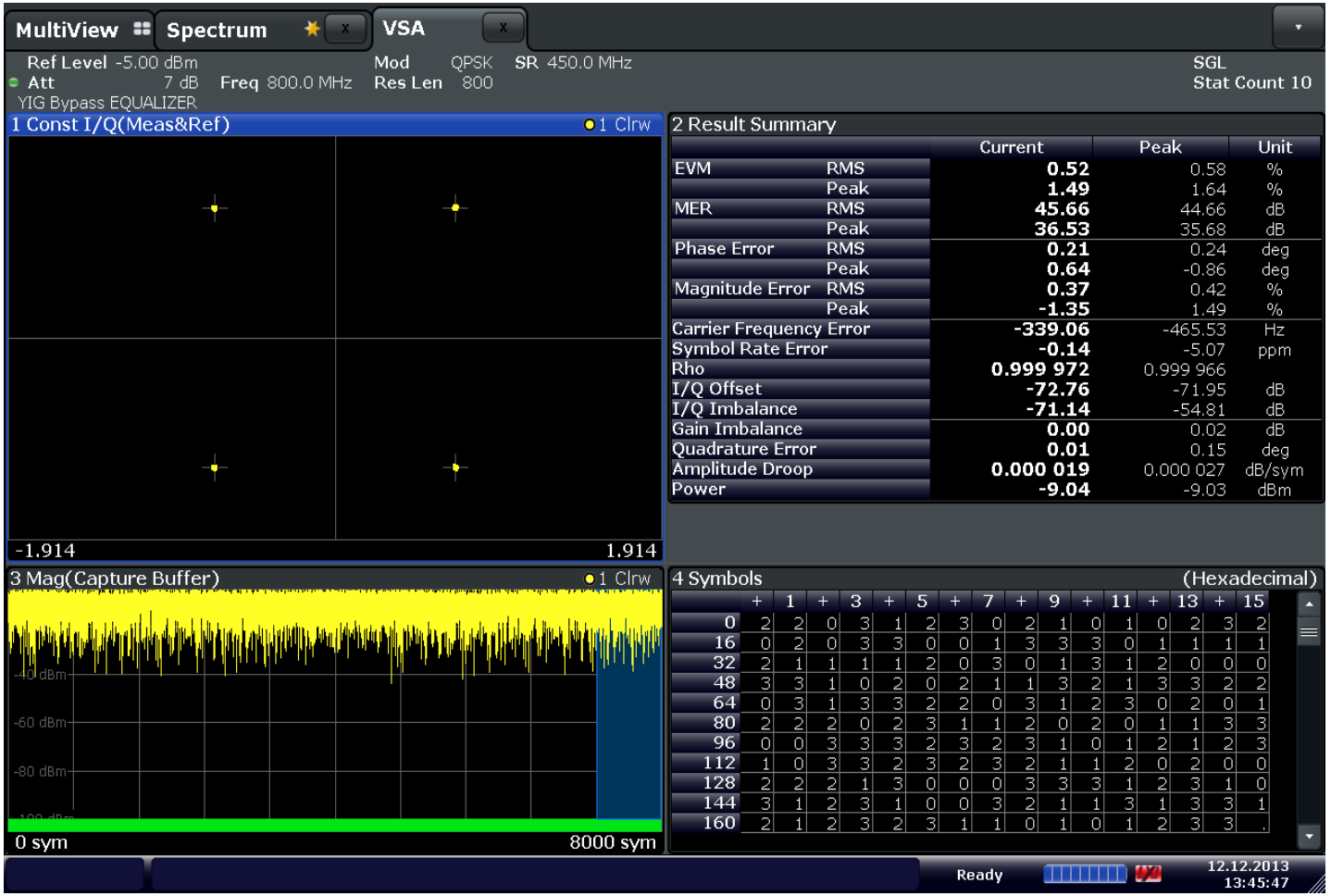

Figure 1. *Demodulation of a QPSK-modulated signal with a bandwidth of just under 500 MHz using an R&S FSW signal and spectrum analyser.*

rent LTE standard uses signals up to 20 MHz wide, which can also be bundled (combined). Ever-wider signal bandwidths are also required in the WLAN standard, and a bandwidth of up to 160 MHz is required in the current IEEE 802.11ac standard. The bandwidth of communications signals via satellite is still around 30 MHz for DVB-S. Signals with a bandwidth of up to 500 MHz are planned in the Ka band for its successor DVB-S2, under the name "DVB-S2 wideband". Even wider signals are used in the microwave links that interconnect mobile communications base stations, for example. The signals of such connections are modulated in the E-band at 71 to 76 GHz with a bandwidth of up to 2 GHz.

The quality of such digitally modulated signals is characterised by values such as the error vector magnitude (EVM) and the pilot-to-data power ratio (total power dynamic range). These values are only determined by demodulating the signals. This requires signal analysers with an analysis bandwidth that is at least as wide as the signal bandwidth.

Fig. 1 shows an example of the demodulation of a QPSK-modulated signal with an R&S FSW signal and spectrum analyser, plus the R&S FSW-K70 vector signal analysis option. Next to the constellation diagram is a table showing the most important quantities for describing signal quality such as the EVM, the phase error and the symbol rate error. The vector signal analysis option makes it possible to demodulate any modulated single carrier up to a bandwidth of 500 MHz and provides numerous other analysis functions, including channel compensation. The signal analysed here has a sample rate of 450 MHz which – with an RRC filter with a rolloff factor of 0.1 – results in a bandwidth of just under 500 MHz.

This short article continues with a summary of the architecture of a current-generation analyser, indicating how it achieves the required bandwidth performance. Click for pdf.

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ADC UNDERSAMPLING REQUIRES WIDE BANDWIDTH

BY IAN BEAVERS, ANALOG DEVICES

Wider frequency communication bands require not only a larger observed bandwidth, but can drive the need for higher full power bandwidth (FPBW) ADCs. Next generation GSPS (Gigasample/sec) ADCs allow GHz sampling into the 3rd and 4th Nyquist band with dynamic range for small signal detection. It is possible to downconvert directly in the ADC by undersampling the IF signal of interest. Higher bandwidth input signals and sample rates allow direct RF sampling of wider band signals and possible reduction of an entire stage in a signal chain for lower system power and simplicity.

ADC undersampling essentially uses a sampling frequency less than twice the maximum frequency component in the signal. To reconstruct the original signal perfectly from the sampled version, the Nyquist-Shannon Sampling theorem indicates that the sample rate must be twice the signal bandwidth of interest.

If BW is the signal bandwidth of interest, then a sample frequency of Fs > 2BW is required. The signal bandwidth can be between DC to BW or from A to B where BW = A – B. So long as this bandwidth does not overlap an ADC's Nyquist band, ½ the sample rate (Fs), undersampling can work for higher signal bands with high FPBW ADCs relative to sample rate.

New GSPS ADCs such as AD9234, AD9680 and AD9625 offer multiple Nyquist band sampling with high dynamic range across wide input bandwidths. Sampling digitization of 500 MHz, 1,000 MHz and even larger segments of spectrum bandwidth in a single Nyquist band helps provide a means to move communication bands higher in frequency beyond the first Nyquist.

Since a direct sampling technique folds signal energy from each zone back into the first Nyquist, there is no way to accurately discriminate the content source from unwanted noise. As a result, rogue energy can appear in the first Nyquist zone, which can degrade the signal-to-noise ratio (SNR) and spurious free dynamic range (SFDR). Using a high order ADC Nyquist band to sample requires strict front-end anti-alias band pass filtering and frequency planning to prevent spectral energy leakage into other Nyquist zones. It ensures unwanted harmonics and signals do not fall into the band of interest after folding down to the 1st Nyquist.

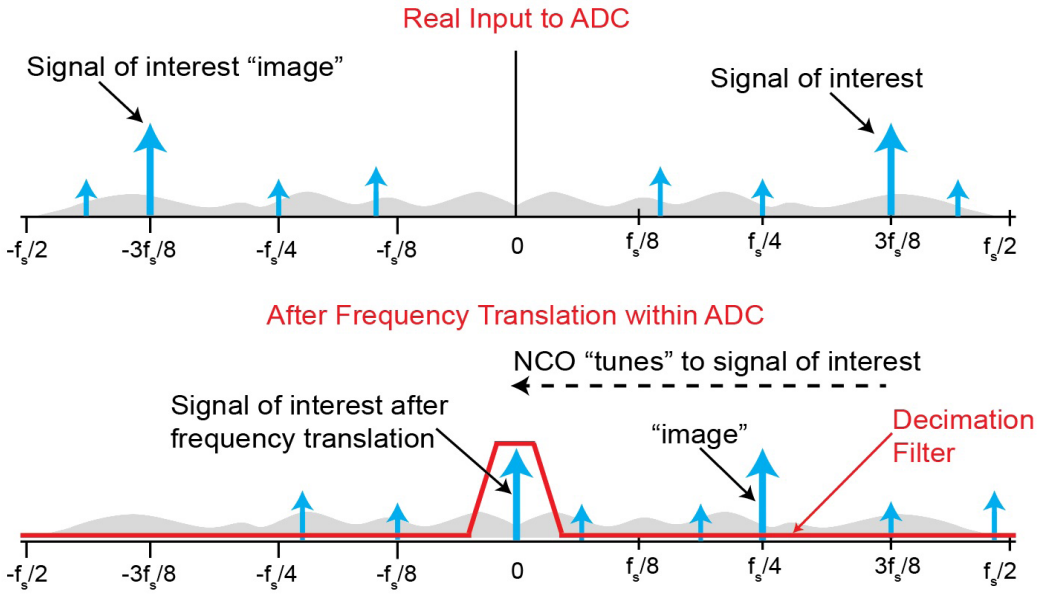


Figure 1. *Wide ADC FPBW allows use of higher order Nyquist bands. Band pass filtering is mandatory to prevent unwanted signal energy from folding back into the 1st Nyquist, impacting dynamic range.*

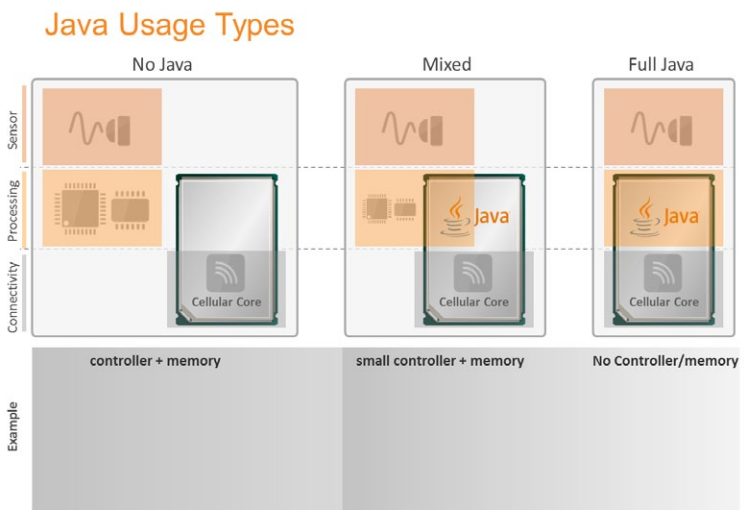
JAVA: THE KEY TO SOFTWARE DEVELOPMENT IN THE INTERNET OF THINGS

By Andrew Pockson, Anglia Components

With a massive developer base, targeted development kits and application enablement platforms, Java is making it easier than ever to develop and prototype robust IoT applications.

There is a common misconception that Java is an operating system. It is much more than that: a programming language and a runtime environment too.

In contrast to other programming languages such as C and C++, Java is compiled into platform independent byte code and interpreted by Virtual Machine (JVM) on whichever platform it is being run. Not surprisingly, it has become the most pervasive open standards programming language in the world, running on billions of devices and machines ranging from mobile phones to enterprise servers to supercomputers. Platform independence and the ability to distribute bytecode over the Web make Java the ideal choice for IoT applications.



By 2012 Java had already become ubiquitous in enterprise applications and mobile devices. That year the platform made its first move in the direction of machine-to-machine (M2M) applications, as Oracle and Qualcomm announced a collaboration that enabled Java Micro Edition software on the industry-leading 3G modem chipset. Nandini Ramani of Oracle presaged a rosy future for the platform, saying: "Having a Java platform across a wide breadth of embedded devices unlocks many new possibilities in the M2M market for developers." This initiative led to Java being used on automotive as well many competing M2M applications, before emerging as the leader in IoT software.

Besides its huge installed base, a further advantage is Java's rich pool of Java developers – around 10million of them at the last count. This is just as well, since according to a recent report (Vision Mobile, June 2014) around 4.5million developers will be working on IoT projects by 2020. Many of the newcomers to IoT will be using Java.

But it is Java's "write once, run anywhere" flexibility that delivers the code portability, increased developer productivity and reduced overall cost of development for IoT.

Java usage cases

A typical IoT "thing" consists of a sensor or actuator, some processing functions and connection to the Internet. This could be implemented with no Java using a relatively powerful microcontroller and memory to store data and code. More usually, a mixed solution is one based on a small controller with memory running Java virtual machines to implement communications protocols, implement security and provide simple and secure application management. It is also possible to implement the entire solution in Java, with the sensor/actuator being the only element in the hardware bill of materials.

This article continues by looking at some of the development product that is available to implement IoT concepts using Java – click for pdf.

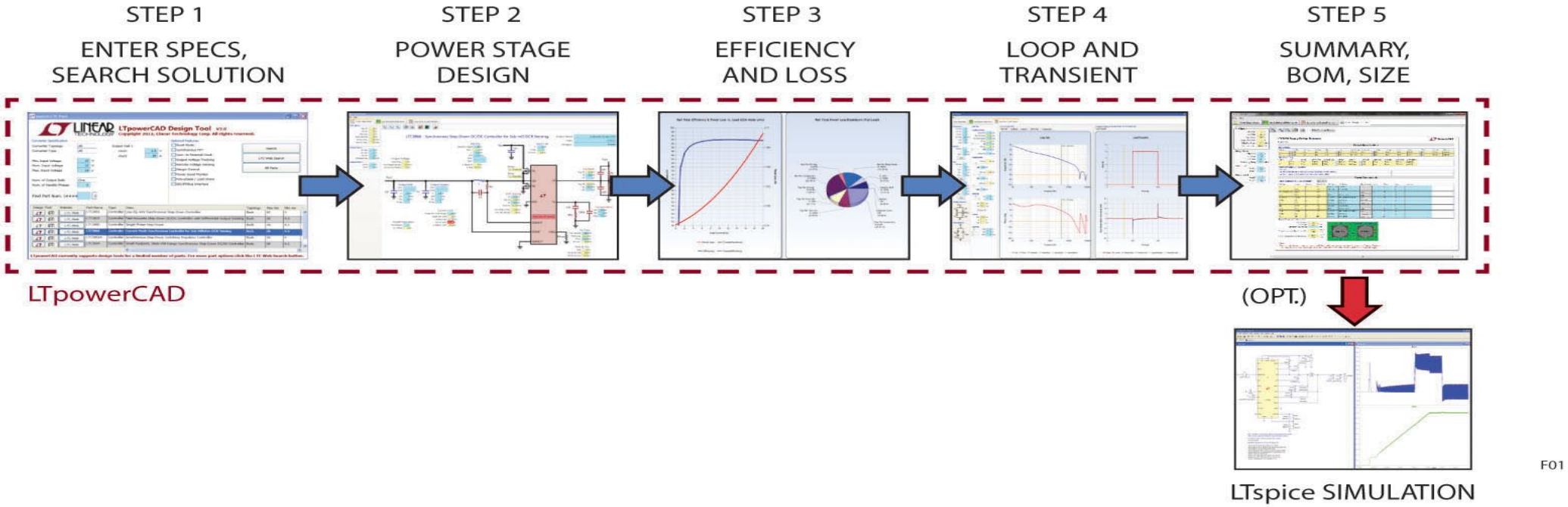
DESIGNING POWER SUPPLY PARAMETERS IN FIVE STEPS WITH THE LTPOWERCAD DESIGN TOOL

By Henry Zhang, Linear Technology

System boards today have an increasing number of power rails and supplies. Since solution size, efficiency, thermal and transient performance are all critical for advanced power solutions, it is more efficient and cost effective to design customised onboard power solutions for a specific application, rather than use commercial power supply bricks.

To system engineers, designing and optimising switching mode power supplies is becoming a more common and necessary task. Unfortunately, this task is often time consuming and technically challenging.

To simplify the design task and improve design quality and productivity, Linear Technology developed its own power supply design and optimisation software tool. LTpowerCAD is a free, downloadable PC-based program. This article explains how to do a "paper design" of switching mode power supply key parameters in a few simple steps with good results.



"Paper design" issues

To design and optimise an onboard power supply, the conventional "paper-design" approach can be difficult and time consuming. After the supply specification is defined, the engineer first needs to select a converter topology, such as a buck converter for voltage step-down or a boost converter for voltage step-up applications. Next, the engineer needs to select a power management IC, either based on past experience or web-search tools. After that, the engineer needs to calculate power component values based on his/her own knowledge or the vendor's data sheet equations. Then comes the choice of power components, such as inductor capacitors and MOSFETs, from the thousands of available parts. The next step is to estimate the supply efficiency and power loss, while ensuring component thermal stress to be acceptable. That's not the end of the story — loop compensation design is another challenging task, since it requires complicated circuit modelling and parameter values beyond the IC data sheet. Finally, the schematic is drawn and the prototype PCB board is sent out for fabrication. Now it's time for the engineer to power up the board to ensure there's not an oscillating output, or overheating. This design process is a challenging one for an inexperienced power supply designer. Even for experienced power designers, the conventional "paper design" approach and trial and error method is time consuming and difficult, and also inaccurate, lacking optimum results. It can take hours, days or even longer.

To save the user time and effort and to achieve a high quality design solution, the software design tool provides a systematic and simple way to enable the design of the key parameters of a power supply in five steps: (1) entering supply specifications and selecting a solution; (2) optimising power stage components with the help of automatic warnings; (3) optimising supply efficiency and power losses; (4) designing loop compensation and optimising load transients; (5) generating a summary report with BOM and PCB size estimation. Figure 1 shows the design flow using the tool.

The detailed design steps can be illustrated with a design example. For instance, an engineer needs to design an onboard supply with the input of 10.8V to 13.2V (12V ±10%) and output of 1.0V with up to 20A current. This is a typical synchronous buck step-down converter. Click the link to follow the example.

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THE TRADEOFF BETWEEN CROSSTALK AND LOSS

BY RANSOM STEPHENS

High Speed Serial standards such as 100G and 400G Ethernet and the OIF-CEI 28G and 56G standard-like "information agreements" try to allot designers as much freedom as possible in how they satisfy performance requirements without sacrificing interoperability.

Newer specifications require more than one stressed receiver tolerance test: a noise tolerance test that focuses on how robust the receiver is to ISI (intersymbol interference), random noise and jitter, and sinusoidal jitter that tests clock recovery and equaliser performance and at least one separate interference tolerance test that probes receiver performance with crosstalk. In the latter, crosstalk is balanced against channel loss in kind of a cool – if arcane – way.

To explain how it works, we need to sort out ICN (integrated crosstalk noise). It doesn't matter whether the signal is PAM4 or NRZ/PAM2. Consider a multi-channel system, like 4 x 25 Gbit/sec for 100 GbE or 8 x 50 Gbit/sec for 400 GbE. Multi-channel systems have crosstalk aggressors for each pair of signal carriers. In Ethernet terminology, aggressors are called "disturbers." The rms near-end and far-end crosstalk (NEXT and FEXT) for multi-channel systems are parameterised by these unwieldy expressions:

$$\sigma_{nx} = \sqrt{2\Delta f \sum_{n=1}^{N} W_{nt}(f_n)\, 10^{-MDNEXT(f_n)/10}}$$

and

$$\sigma_{fx} = \sqrt{2\Delta f \sum_{n=1}^{N} W_{ft}(f_n)\, 10^{-MDFEXT(f_n)/10}}$$

The sum is carried out over all pair-wise combinations, Δf is the frequency step over which the crosstalk is summed, W is a weighting function that models the receiver's frequency response, and MDNEXT and MDFEXT are the equivalent crosstalk losses in decibels. ICN is then given by:

$$\mathrm{ICN} = \sigma_{nx} = \sqrt{\sigma_{nx}^2 + \sigma_{fx}^2}$$

You need the differential S-parameters of the whole system—including scattering between separate channels—to calculate or simulate ICN.

Let's go back to design flexibility.

One approach at 28.5 Gbits/sec requires levels of ICN that depend on the channel insertion loss measured at the signal's fundamental harmonic frequency. Figure 1 shows the range of compliance and the tradeoff between insertion loss and crosstalk.

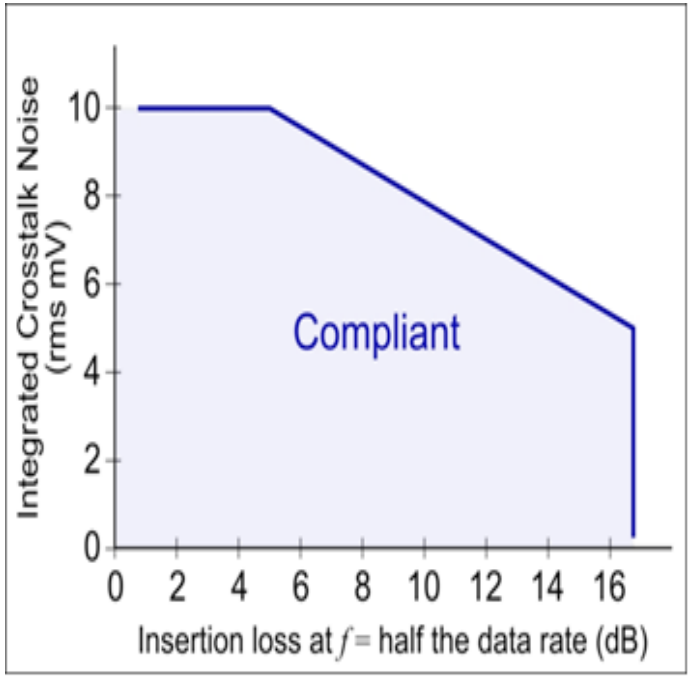


Figure 1. *Balancing crosstalk, ICN, against insertion loss.*

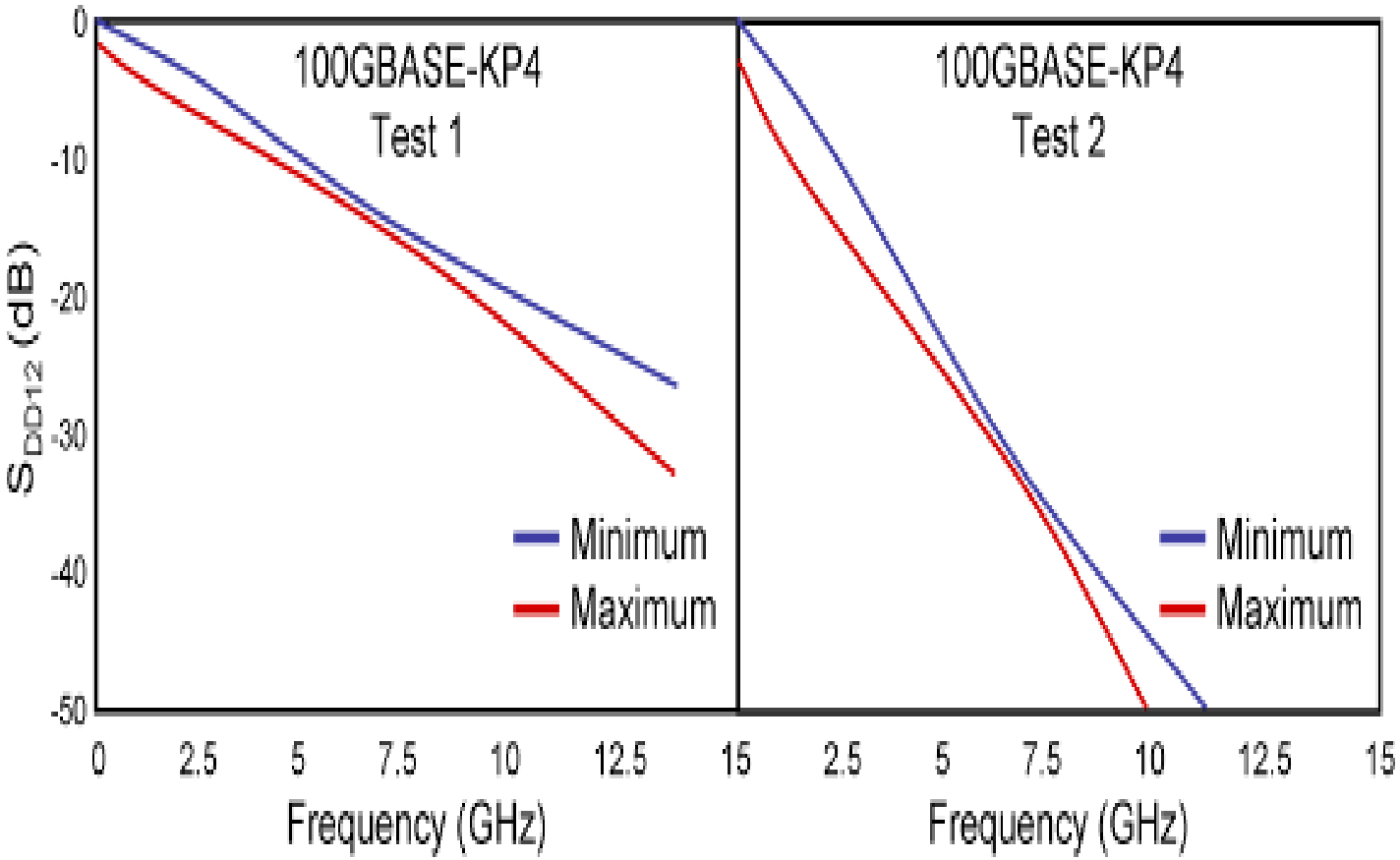


Figure 2. *Masks for the frequency response of low and high loss channels (Courtesy of Tektronix Instruments).*

Emerging specifications such as 400G require that receivers pass two separate interference/crosstalk tests: one with a high loss channel and low crosstalk and one with low loss and high crosstalk. The channel loss requirements are specified by differential frequency response masks, like those in Figure 2. The high and low crosstalk conditions are specified implicitly by requiring COM (channel operating margin) < 3 dB for both tests.

COM is essentially the ratio of the signal amplitude to the combination of all signal impairments, including crosstalk and channel loss—like a generalised signal-to-noise ratio. COM is calculated from the combination of S-parameters, models of the transmitted and received signals, random and deterministic jitter, and voltage noise, and the effects of equalisation schemes at both the transmitter and receiver.

Both the low loss test 1 and high loss test 2 require COM to be less than but close to 3 dB—the performance spec for the channel is COM >3 dB, so this counts as maximum, even extra stress. With the same COM value for both tests, the increased channel loss of Test 1 implies a decrease in crosstalk and, for Test 2, vice versa.

By specifying a minimum compliant COM, standards provide flexibility in how designers budget the combination of ISI, random noise and jitter, and crosstalk. By combining that spec with two channel loss performance criteria, the flexibility is reduced but interoperability is enhanced.

2016 PREDICTIONS FOR MIXED-SIGNAL IC DESIGN

By Hao Fang, Cadence

The latest advances in automotive and Internet of Things (IoT) devices continue to drive the complexity of today's mixed-signal designs, significantly challenging mixed-signal verification.

Engineers require solutions that span from transistors to chips to systems, and they also need better ways to improve productivity. This article will examine the key trends, challenges, and emerging solutions in mixed-signal system design enablement, focusing on mixed-signal verification.

Taking a system-level view of automotive design

Approximately 85% of SoC design starts are mixed-signal designs, according to IBS, and many of them also require low power consumption. Automotive designs provide a good illustration of an industry where engineers are facing more system-level design challenges. In years past, a typical automotive design would have simple microcontrollers and a single sensor. Now, particularly with the rise of autonomous driving, infotainment systems, and advanced driver assistance systems (ADAS), vehicles have multiple sensors and MCUs that may need to talk to each other.

At the device level, these chips must be simulated, and verified that they can operate reliably under extreme environmental conditions. At the system level, the vehicle must be designed so that it will respond to all of the sensor inputs safely. For example, engineers must ensure that sensor data can be aggregated and analysed to present an accurate picture of what is happening, whether the vehicle needs to detect a jaywalking pedestrian or an errant lane change by another car. IP, design tools, and other components in the supply chain must be certified to meet vehicle functional safety standards, such as ISO 26262.

Power hasn't been a big concern in automotive design, as the vehicle battery has generally been sufficient to provide the power needed by in-vehicle electronics. However, cars now commonly contain hundreds of sensors, feature in-vehicle connectivity via wireless protocols, and also boast redundant sensors and systems for reliability. More low-power design techniques need to be incorporated to reduce the total power consumption of the electronic system. The power distribution system, particularly for electric cars, might at some point require a redesign in order to provide enough power to accommodate all of these sources.

One surprising trend that is underway for the automotive industry is a shift to advanced-node SoCs. Larger process nodes have long been sufficient for automotive SoC designs. However, since automotive sensors are aggregating so much more data these days, powerful processors are needed to analyse this data and make real-time determinations. What's more, the volume of data is likely to grow—future cars will probably need to be able to communicate with other cars, for example. Advanced-node chips would provide the processing speeds to support this.

Lowering power of IoT designs

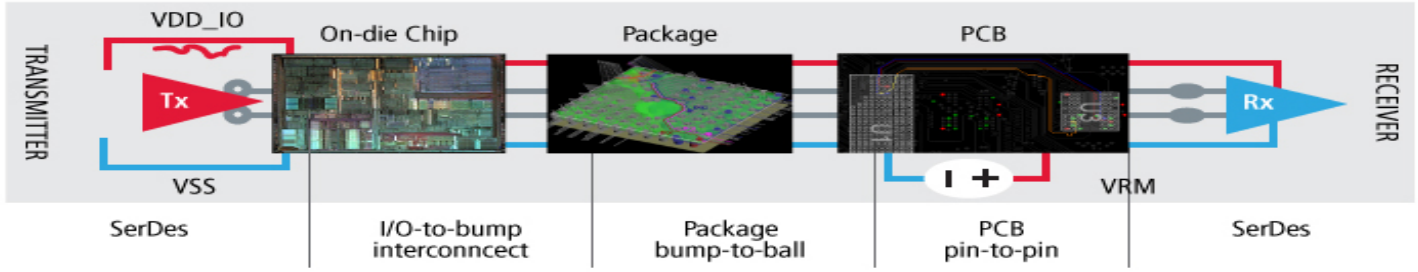
IoT designs encompass a broad array of end devices, all requiring connectivity. Power consumption is an extremely critical element in field sensors and wearable devices. To meet the stringent low-power requirements, many engineers are turning to techniques such as ultra-low power design, via sub-threshold CMOS design, and the integration of elaborate power-management control systems. These techniques require better characterisation of devices at low voltage levels, with special attention paid to process variations and leakage power. Foundries are developing processes specifically targeting ultra-low power designs.

Energy harvesting also presents a promising future option. The photovoltaic method is currently the most common method. Energy harvesting from radio or sound waves remains in the research phase. Currently, the amount of power being harvested from those new methods is fairly low and may not be sufficient [even] for ultra-low power designs.

Like automotive, IoT designs, too, are driven by large volumes of data that need to be aggregated and analysed. In IoT gateways and cloud servers, performance and connectivity features are critical to success. Advanced-node processes are a playing an important role in providing sufficient computing power. Foundries are continually driving towards sub-10nm process nodes. However, advanced-node processes can only push things so far. Many engineering teams are also tapping into 2.5D and 3D technologies to combine chips with different technologies through advanced packaging. This not only extends Moore's Law, but also can take advantage of multiple process nodes to optimise device performance.

All of these methods and technologies lead to more complex verification of chip, package, and board—and a need for better analysis tools to ensure signal integrity and power integrity, model thermal effects, and more.

It's also more important to look at a design holistically... *article continues with observations on the need to simulate the chip with the package and the board as an entire system. Click for pdf*



There is an increasing need to verify designs holistically, as end-to-end systems, as the continuation of this article explains.

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HOW TO COMBINE VOLTAGE AND CURRENT REGULATION

By Matthias Ulmann, Texas Instruments

A typical power supply provides a fixed output voltage and a maximum current. The maximum output current can be fixed or adjustable, dependent on the device. Switchers with integrated FETs have, in general, a fixed current limit: controllers for external FETs offer the possibility to set the current limit externally. In both cases the voltage drop across the FET (drain-source) or a shunt is monitored and compared to a reference voltage. If the voltage is higher than the reference, the power supply may take different actions, depending on the implementation of the overcurrent protection.

One method is to switch off the converter for a certain time and then start up again. During the off-time, the output voltage drops and no current is supplied to the load. This is the typical behaviour of a simple overcurrent protection. The second method is to switch off the FET when the adjusted peak current (peak voltage on the FET or shunt) is reached. The converter keeps on switching: only the on-time is reduced. This behaviour is known as "cycle-by-cycle current limit". If the load is increased further, the output current remains constant and the voltage decreases. With this method a form of output current control can be implemented – this is needed, for example, for highly capacitive loads during startup. Using this approach, peak loads do not cause switch-off of the supply.

This form of current limit has limited accuracy, a tolerance of at least ±10% of the reference, therefore precise current control such as is needed for battery charging is not possible. For this kind of application, voltage and current need to be kept within a tight tolerance band to ensure a long lifetime of the battery and to avoid any damage due to overcharging. Therefore the controller has to precisely limit the output current as well as the output voltage. This article describes how to nest voltage and current regulation with a standard PWM controller for high accuracy. The regulation of both parameters is not fixed to the output. Of course, you can also limit the input current or, like in this example, the charge current of the output capacitor. In practice, each current and voltage of a converter which can be measured can be controlled.

Current and voltage measurement

The Sepic converter used in this example has to supply large pulsed loads. As the current of the converter's source is limited, the pulsed currents have to be supported by a large output capacitor. At the same time the input current needs to be limited so that the source is not overstressed. Figure 1 shows the simplified schematic of the converter with the LM5001 integrated boost converter, used in Sepic configuration, and a large electrolytic capacitor at the output.

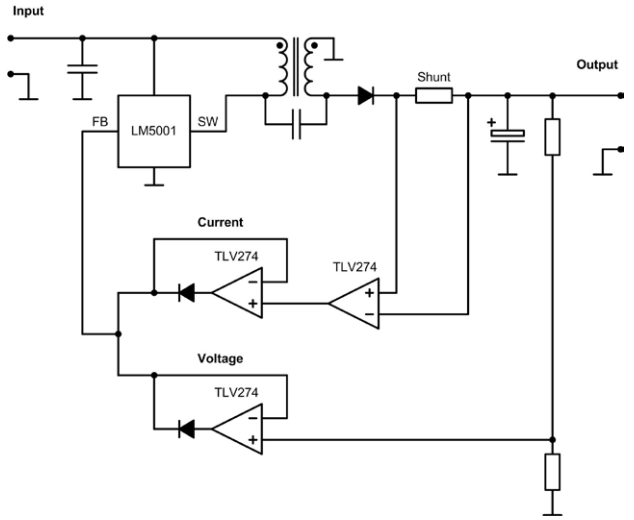
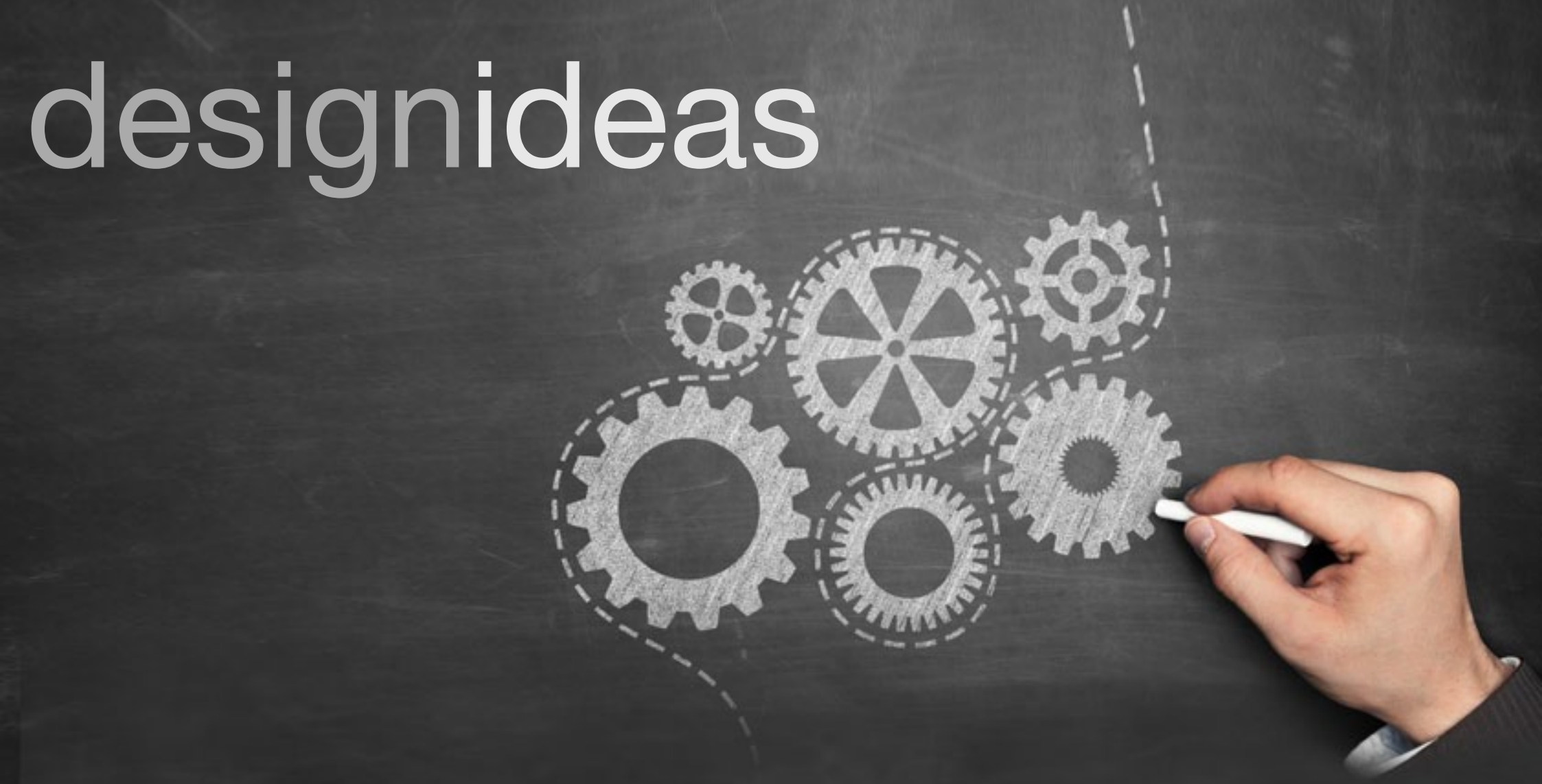


Figure 1. *Simplified schematic*

This article continues, expanding on the feedback paths used to ensure voltage and current regulation – click the link for full pdf.

designideas



- A faster PWM-based DAC
- AVR takes under 1 µsec to process quadrature encoder

A faster PWM-based DAC

By Dusan Ponikvar

When you need an analogue output from a microcontroller that does not have a digital-to-analogue converter (DAC), you can connect an external DAC chip. But for a cheaper solution, use a pulse-width modulated (PWM) output and add a low-pass filter (LPF) to extract its average value, which equals the duty cycle of the PWM signal.

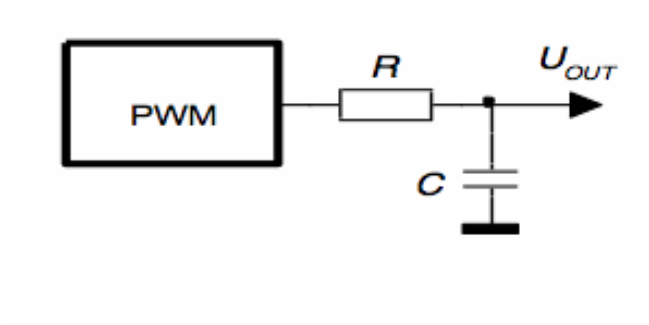


Figure 1. *An RC LPF extracts the average value of a PWM signal*

The RC filter removes the non-DC components; what remains is the average signal U_{OUT}. If the period T of the PWM signal equals 63 clocks, the signal U_{OUT} can have one of 64 discrete DC values (0 to 63, six-bit resolution).

The time constant τ of the low-pass RC filter must be big enough to smooth the output signal U_{OUT}. The ripple, ΔU_{OUT}, should be less than one least significant bit (LSB). The worst case occurs with a duty cycle of 50% (Figure 2). If τ is much bigger than the period T then the capacitor charging current I_C and the change ΔU_{OUT} can be approximated as:

$$I_C \approx {V_{CC}}/{2R} \quad \text{and from:} \quad C\,\Delta U_{OUT} = I_C\,{T}/{2} \;\rightarrow\; \Delta U_{OUT} \approx {V_{CC}\,T}/{4RC}$$

For a 6-bit DAC, ΔU_{OUT} should be less than $V_{CC}/64$, requiring a filter of $\tau = RC \geq 16 \cdot T$.

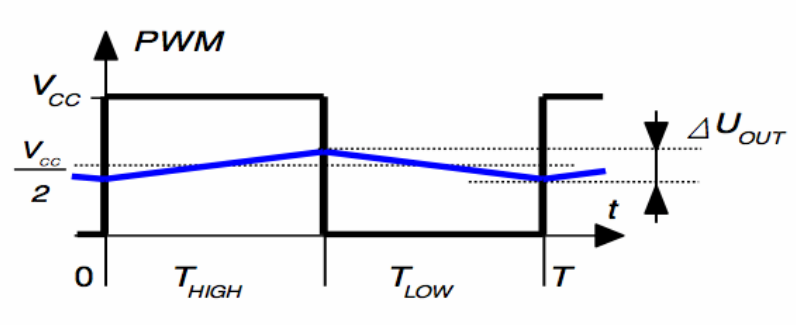


Figure 2. *The filtered output (blue) should have less than one LSB of ripple.*

Some practical numbers: low-power microprocessors often use a crystal oscillator of 32768 Hz, and this clock signal is used for the PWM block. With 6-bit PWM, the period T is 64/32768 ≈ 2 msec, necessitating a time constant of 32 msec. One has to wait 5τ (160 msec) for a 6-bit converter to settle. Slow. This Design Idea explains how you can speed things up.

PWM blocks in microcontrollers can usually generate more than one PWM signal. Consider summing outputs from two PWM based 3-bit DACs (DACH and DACL), where the output of DACL is reduced to one-eighth amplitude before adding. The resulting signal acts as a 6-bit DAC, with an important advantage over the simple version: the period T is

only eight clock periods for the same resolution, and the required time constant τ is 1/8 of the previous, speeding up settling time by a factor of eight. Such an arrangement is easy to implement with resistors in the RC filter for two PWM signals (PWMH, PWML):

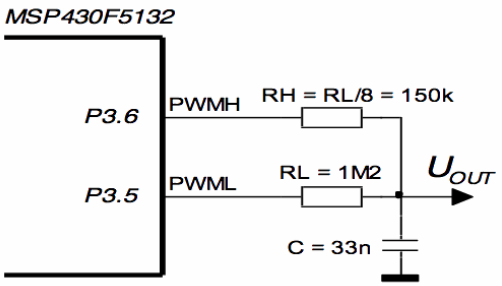


Figure 3. *Combining two PWM-based DAC outputs*

The output signal U_{OUT} is given by:

$$U_{OUT} = \left(DUTY_{PWMH} + {}^{DUTY_{PWML}}/_{8}\right) \cdot \frac{V_{CC} \cdot R_L}{R_H + R_L}$$

This technique has been implemented in a TI MSP430F5132 microcontroller:

```
  // configure PWM - 32 kHz / 8 = 4 kHz :: 6 bit in two
PWMs, done only once on power-up
  TA0CCR0 = 7;
// count up to 7 (including)
  TA0CTL = TASSEL__ACLK | MC_1 | TACLR;
  TA0CCR1 = 0;          TA0CCTL1 = OUTMOD_6;
// toggle/set
  TA0CCR2 = 0;          TA0CCTL2 = OUTMOD_6;
// toggle/set
  // use :: write to PWM block to achieve the desired
DAC output
  DAClevel++;
// next DAC level, DAClevel is a char
  TA0CCR1 = (DAClevel >> 3) & 7;
// set PWMH: MSB 3 bits
  TA0CCR2 = (DAClevel         ) & 7;
// set PWML:  LSB   3 bits
```

Figure 4. *Code to initialise & write to a 6-bit (3+3) PWM-based DAC*

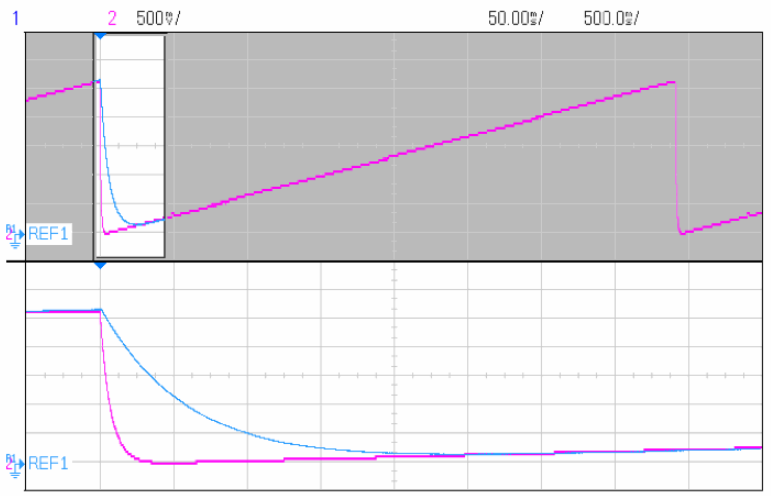


Figure 5. *Measured outputs from 6-bit PWM-based DACs; Blue: implementation as in Figure 1 (160 msec settling); Violet: implementation as in Figure 3 (20 msec settling)*

A 7-bit DAC can be implemented using 1% resistors. This time, two PWM signals are used to make two three-bit DACs, totalling six bits, and the MSB is simply set to 0 or 1 at P3.7.

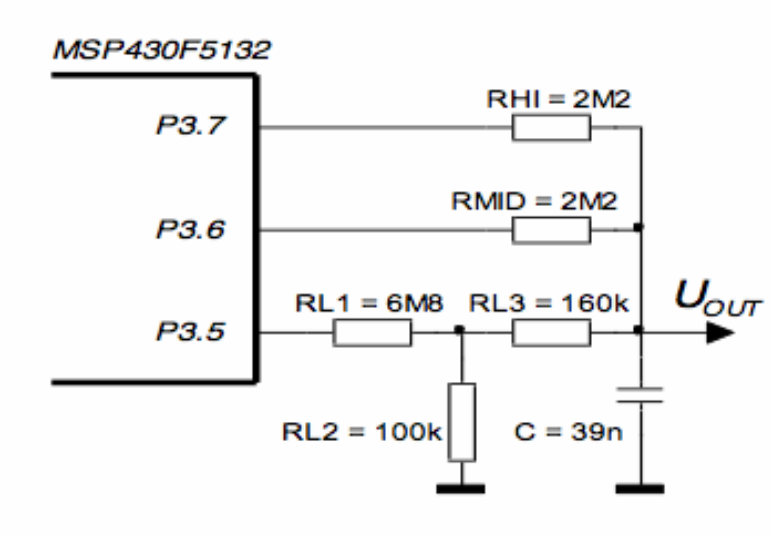


Figure 6. *An implementation of a seven-bit PWM-based DAC*

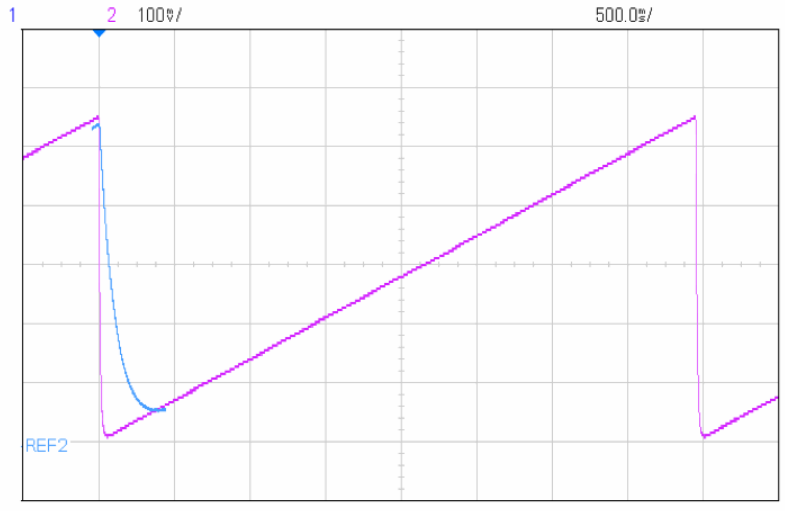


Figure 7. *Measured output of Figure 6 circuit; note the good linearity.*

```
// configure PWM - 32 kHz / 8 = 4 kHz :: 7 bit in two
PWMs and one digital pin, done only once on power-up
// is the same as given in configure section in figure 5

// use :: write to Timer comparators to achieve the
desired DAC output
DAClevel++;
// next DAC level, DAClevel is a char
TA0CCR1 = (DAClevel >> 3) & 7;
// set PWMH, MSB, 3 bits
TA0CCR2 = (DAClevel     ) & 7;
// set PWML,  LSB,  3 bits
if (DAClevel & BIT6) P3OUT |= BIT7; else P3OUT &=
~BIT7;      // set MSB, no PWM
```

Figure 8. *Code to initialise & write to a 7-bit (3+3+1) PWM-based DAC*

The speed improvement here is even greater. A simple PWM DAC would have a period of 128 clock periods (128/32768 s^{-1}= 3.9 msec), resulting in τ of 32·T = 125 msec and a settling time of 5 · 125 msec = 625 msec. Figure 7 settles in 40 msec — 16× faster. A higher-order LPF would also help to reduce settling time. *See next page for references.*

About the author

Dusan Ponikvar is assistant professor at University of Ljubljana, Faculty of Mathematics and Physics (Slovenia). He teaches courses in Electronics (analog electronics, operational amplifiers, transfer functions, stability, modulation and demodulation, digital electronics, regulation basics, noise), Data acquisition and processing (data acquisition using a PC, Labview, filtering FIR and IIR, FFT), The use of microprocessors (microprocessor data processing in physics experiments); and is involved in the design and construction of electronic instruments.

References:

Stephen Woodward:
Fast-settling synchronous-PWM-DAC filter has almost no ripple
David M. Alter:
Using PWM Output as a Digital-to-Analog Converter on a TMS320F280x Digital Signal Controller
Mike Mitchell:
Using PWM Timer_B as a DAC
Amar Palacherla:
AN538: Using PWM to Generate Analog Output

AVR takes under 1 µsec to process quadrature encoder

By Ioan Ciascai & Liviu Viman

Reading quadrature encoder signals at high speeds (e.g., 1 MHz, or, 1 m/sec with a resolution of 1 µm) often requires dedicated hardware. This Design Idea shows a simple scheme to accomplish this function using only an ATtiny2313A AVR microcontroller. Of course, the microcontroller can also be connected to other devices via the serial interface, or the measured position can be displayed on a local LCD, which could be connected to port PB. Additionally, one or more LEDs can be added to signal error conditions.

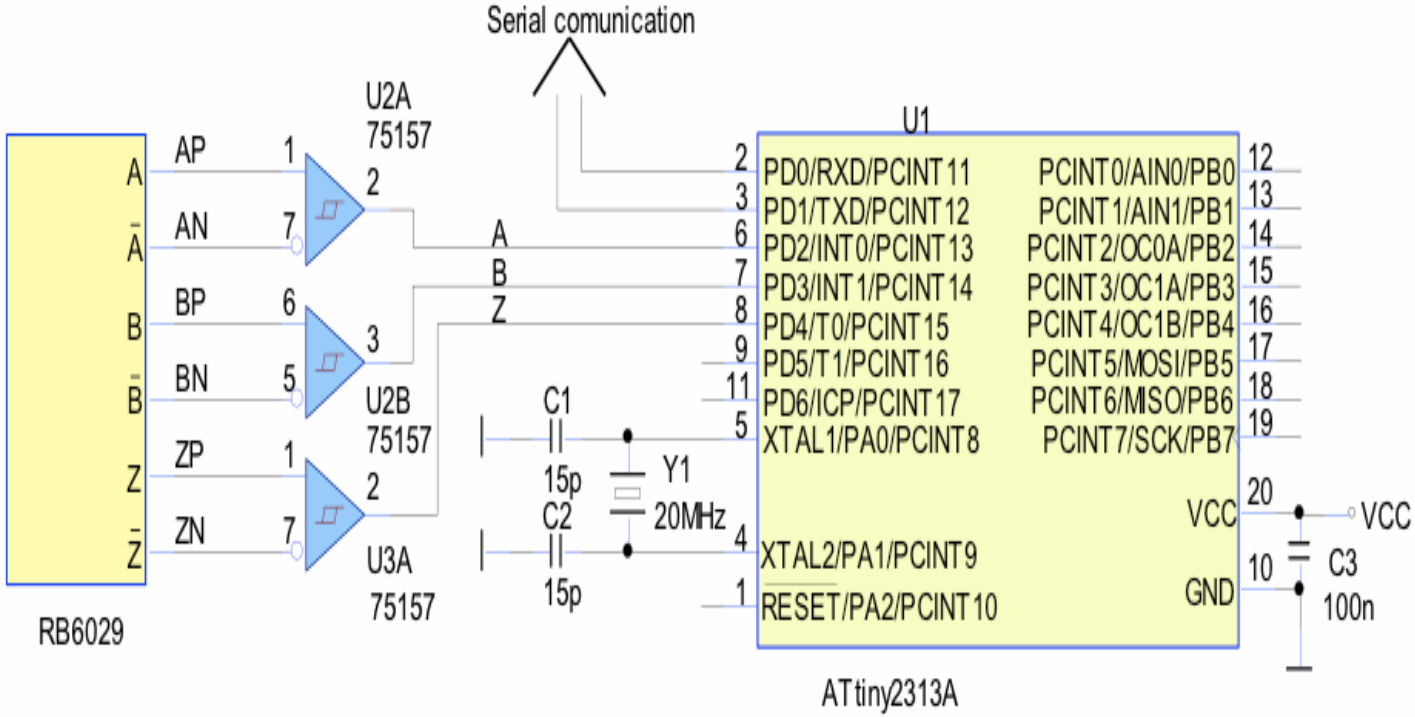


Figure 1. *Reading quadrature signals with ATtiny2313A; the Z index signal is optional.*

In this implementation, the interrupt handler is very important. It reads input signals A and B in less than 1 µsec. Differential signals AP/N and BP/N are processed by SN75157 receivers, un-needed if your encoder outputs logic-level signals.

The processor is configured to generate an interrupt for any change of port PD pins. This interrupt is the last in the table of interrupt vectors, and hence can dispense with the jump instruction, resulting in a reduction in the interrupt service time of 2-3 clocks (100-150 nsec).

An XOR operation between previous and current signals ($A_{old} \oplus B_{new}$ or $A_{new} \oplus B_{old}$) determines if the current position has incremented or decremented from the previous. A_{old} and B_{old} are the A and B signals before changing state, and A_{new} and B_{new} are the values after the interrupt. The interrupt handler is in the *PCIsubroutine1.txt* file.

The execution time of the interrupt handler is 800-850ns (16-17 clocks). To minimize the execution time of the ISR, some registers have been dedicated to it and must not be used by the main program:

- R10 to save SREG and test for activation of new interrupt
- R11 and R12 for the new and old states
- R24 and R25 for position transducer

To calculate the current position requires only one clock cycle. The downside is that the position can only have 65536 values. You can determine the position using 3 or 4 bytes, in which case the subroutine execution time increases to 18-19 cycles from adding the necessary instructions (use the register pair R24, R26, R28, or R30).

The interrupt handler checks for a new interrupt before exiting the current ISR. This case is signalled by setting bit T in SREG. Implementing this check, the execution time increases by 3 cycles. We have tested the operation of the subroutine using an RB6029 (4,000 pulses per rotation) at maximum speed, with no errors detected.

Before activating interrupts, the PCIE2 value must be placed in register R12 (read PIND register before enabling PCINT2 interrupt and SREG –I flag is set).

If you want to use the Z index signal, the position will be stored in three registers as 1,024,000 values (4,000 counts/rotation; 256 rotations). The interrupt handler to read the data is more complex, as seen in *PCIsubroutine2.txt.* Length is 19 cycles, or 20 cycles when the current position is incremented when Z is active.

If the Z index is active, we clear the angular position, increment the revolution count, and check that the previous angular value was 3,999. In this subroutine, three errors are detected: one for an overlapping new interrupt (as in the previous case), and two related to the Z index (checking the correctness of the previous angular position). Error counter registers rerr1, rerr2 and rerr3 should be defined by the user. To initialise the system, run *InitIndexZ.txt*, which waits for Z to be active.

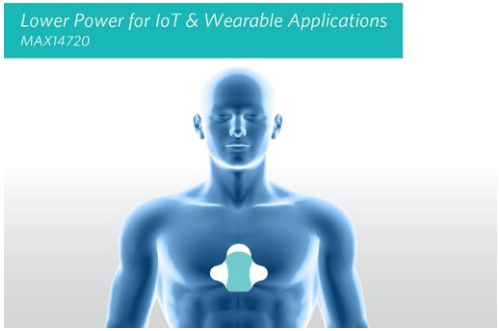
Download the program source files.

productroundup

productroundup

PMIC for wearables, with battery 'seal'

Maxim Integrated's MAX14720 power management chip runs from a primary cell while extending battery and shelf life; intended applications include medical/fitness and Internet of Things (IoT). The PMIC is designed for non-rechargeable battery (coin cell, dual alkaline) applications where size and energy efficiency are critical. An electronic 'battery seal' extends shelf life by effectively disconnecting the battery prior to initial power-up. The IC integrates five discrete devices—power switch, linear regulator, buck regulator, buck-boost regulator, and monitor.



Complete article, here

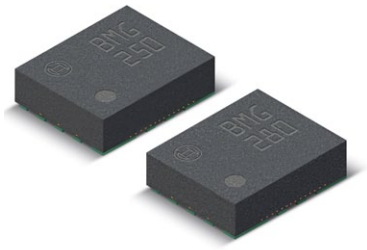
Accurate optical heart rate monitoring

Silicon Labs has introduced an optical heart rate sensing solution designed to reduce the cost and complexity of wrist-based heart rate monitoring (HRM) applications. The Si1144 HRM is an all-optical (transconductance) measurement device that integrates a single (green) LED – there is no resistivity measurement path – that Silicon Labs says can yield HRM results of comparable accuracy to a chest-strap-based monitor. The device includes a low-power optical sensor module with an EFM32 Gecko microcontroller (MCU) running Silicon Labs' own HRM algorithm.

Complete article, here

Accelerometers/gyros for portable products

Bosch Sensortec has announced uprated intelligent accelerometers and high performance gyroscopes; this generation of motion sensors is configured around the needs of embedded intelligence in smart phones and wearables, with extended battery life time. The devices cover a wide range of requirements, from low power consumption for always-on applications such as step counting, to high performance optical image stabilisation (OIS). BMA422 and BMA455 are intelligent three-axis accelerometers: BMG250 and BMG280 are gyroscopes that combine low noise, low TCO and high bias stability, claiming the lowest power consumption of any standalone gyroscope.



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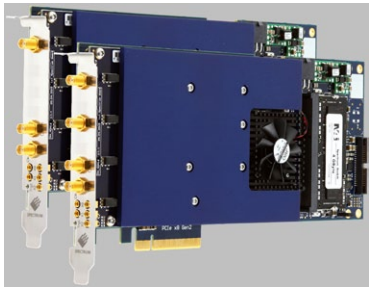
Arbitrary waveform generators run at 1.25 Gsample/sec, 16-bit

Spectrum has added two arbitrary waveform generators (AWGs) that offer one or two channels each capable of outputting electronic signals at rates of up to 1.25 Gigasamples/second with 16-bit vertical resolution, generating high frequency signals up to 400 MHz. The instruments can be used to generate almost any waveform, for stimulating electronic devices such as amplifiers, filters, receivers, and digital interfaces. Waveforms can be acquired from a digitiser or other instrument and loaded into the AWG, or designed mathematically or via tools such as LabVIEW and MATLAB.



Complete article, here

productroundup

15W dual mode wireless charging platform

Providing compatibility for the latest quick charging devices, Semtech's TS80K wireless charging ICs support WPC Q1.2 and PMA SR1E medium power 15W standards. These dual-mode Wireless Power Consortium (WPC) Qi 1.2 and AirFuel Alliance (PMA) SR1E medium power 15W capability join the TS80000 wireless charging range to support the growing market of portable electronics with increased battery capacity. The TS80K family of solutions can support both receiver and transmitter applications with complete reference designs and evaluation kits.

Complete article, here

USB 3.0 & 802.11ad reference design

SiBeam, a Lattice Semiconductor company, has disclosed a USB 3.0 adapter reference design supporting the IEEE 802.11ad wireless standard (also known as WiGig) for wireless connectivity at gigabit per second speeds over the 60 GHz frequency band. Enabling OEMs to build single-band 60 GHz or multi-band USB adapter accessories for laptops and desktops, this USB 3.0 adapter reference design (part number SK65011U) includes the SB6501, an 802.11ad MAC/baseband chip, and the Sil6312, a 60 GHz RF chip with on-package phase array antenna. It can interoperate with Qualcomm Atheros' multi-band access point solution.

Complete article, here

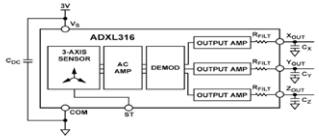
Wireless user-authentication platform for IoT-device security

STMicroelectronics and ClevX have co-operated to offer a technology that allows smartphones and wearables to authenticate with secure IoT devices via Bluetooth Smart: the platform comes with jointly-authored reference designs for secure portable storage media using ST's BlueNRG chips and ultra-low-power STM32L0 MCUs. Users can interact with secure portable storage (full-disc, XTS-AES 256-bit encryption) from their smartphones or wearable devices where all user data on the drive is encrypted and can be locked/unlocked using single- or multi-factor authentication. ST and ClevX have reference designs for secure portable storage media, including Flash, hard-disc, and solid-state disc drives; the designs are available for licensing and partnerships, including both ST/ClevX-based hardware and firmware in addition to the related smartphone and wearables apps.

Complete article, here

3-axis ±16g accelerometer for motion and tilt sensing

Analog Devices has added to its MEMS accelerometer offering, aimed at low-power and cost-sensitive applications such as mobile devices, gaming systems, disc drive protection, image stabilisation, active noise control (ANC) and sports/health devices. ADXL316 is a small, thin, low power, complete 3-axis accelerometer with signal conditioned voltage outputs, on a single monolithic IC. The product measures acceleration with a minimum full-scale range of ±16 g. It can measure the static acceleration of gravity in tilt-sensing applications, as well as dynamic acceleration resulting from motion, shock, or vibration.



Complete article, here

productroundup

Evaluation board for GaN power FET try-out

GaN Systems (Ottawa, Canada) has configured a half-bridge evaluation board to demonstrate its GaN enhancement mode power transistors in real power circuits. The fully functional GS66508T-EVBHB Evaluation Board can adopt any half-bridge-based topology, including synchronous boost and buck conversion modes, as well as pulsed switching to evaluate transistor waveforms. The development kit comes with full documentation, including bill-of-materials component part numbers, PCB layout and thermal management, and a gate drive circuit reference design.

Complete article, here

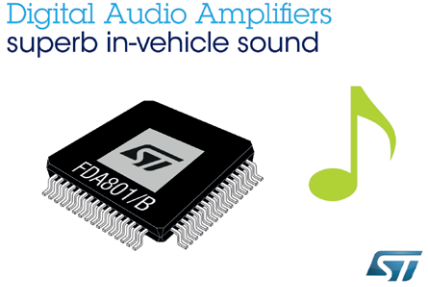
60A digital PoL DC/DC can parallel to 480A

In a compact LGA package enhanced for thermal performance, and aimed at ICT, telecom and industrial applications, Ericsson's 60A 3E* digital point-of-load (POL) DC/DC power module, the BMR466, is designed to power microprocessors, FPGAs, ASICs and other digital ICs on complex boards. Offering small footprint, high stability, advanced loop compensation and advanced thermal characteristics, up to eight of the fully regulated 60A (maximum) POL converters can be connected in parallel to deliver up to 480A in multi-module and multi-phase systems.

Complete article, here

Class-D digital PAs for in-car audio

ST's latest audio power Amplifiers for car audio, the FDA801 and FDA801B 4-channel class-D amplifiers with digital input convert the digital audio source directly into high-quality sound. The digital input gives immunity to GSM noise, improves sound quality, saves component costs, and simplifies system design. ST introduced the first class-D digital-input automotive-audio amplifiers in 2012, and is now moving forward with its new and improved second generation that will be soon completed with pin-compatible ICs in various multi-channel configurations.



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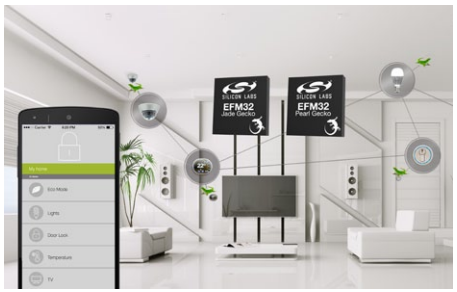
IoT security addressed by low-power MCUs

Differentiating its EFM32 Jade and Pearl Gecko microcontrollers in the marketplace of MCUs for internet-of-things nodes, Silicon Labs cites the presence of hardware cryptography functions together with a range of low-power and sleep modes that, the company says, goes beyond what is offered by other ICs. The hardware cryptography blocks add to the number of functions that the chip can perform without waking the ARM cortex M3/M4 cores from sleep; these include making measurements and carrying out communications operations, and are a cornerstone of the low-power claims made for the chips.



Complete article, here

productroundup

Serial-to-WiFi board for IoT deployment

Distributor Alpha Micro has the xPico Wi-Fi SMT board with u.fl and on-board antennas, that converts serial ports to Wi-Fi connections to simplify the development of large scale IoT applications. By Lantronix, the xPico Wi-Fi SMT embedded device server allows rapid implementation of Wi-Fi connections and wirelessly connected IoT devices that can be monitored via a mobile device, tablet or PC. The device adds a completely integrated on-board antenna with the option to use a u.fl antenna to give additional flexibility and enhanced performance.

Complete article, here

Ethernet PHY over UTP for automotive, industrial

Microchip's KSZ8061 Quiet-WIRE technology 10/100BASE-TX Ethernet physical-layer transceivers provide reduced line emissions and superior receiver immunity over unshielded cabling, meeting automotive and industrial EMC requirements. The KSZ8061 single-chip 10BASE-T/100BASE-TX automotive- and industrial-grade Ethernet physical-layer transceiver is designed for data communication over low-cost Unshielded Twisted Pair (UTP) cables. It is the first of a family based on the patented and programmable Quiet-WIRE enhanced EMC technology, providing reduced line emissions and superior receiver immunity performance.

Complete article, here

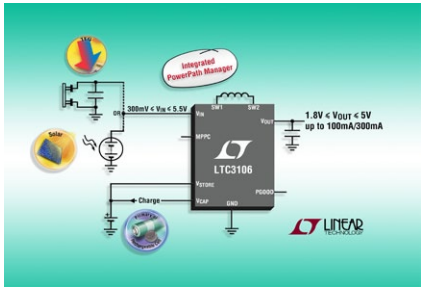
FTDI Kickstarter Project: Arduino UNO R3 compatibility

FTDI Chip says it is, "experimenting with how to bring new solutions to market", with its latest product, NerO, being introduced on KickStarter. The objective of NerO is to deal with the fundamental drawbacks of the widely-used Arduino UNO R3. The UNO R3 compatible board supports higher current demands as well as offering other useful additional features. It is capable of supplying a full 1A with its temperature being well below 100°C at maximum load. This Arduino UNO R3 compatible board covers an input voltage of 7V to 20V (with 9V or 12V recommended). It is supplied with FCC and CE certification. Placed in an attractive price bracket (under $20), NerO has a 16 MHz ATmega328 microcontroller with Optiboot bootloader. FTDI's FT231XS takes care of USB connectivity providing more reliable communications, with FTDI's drivers and support.

Complete article, here

Energy-harvesting buck/boost DC/DC starts from 300 mV

LTC3106 is a highly integrated, 1.6 µA quiescent current, 300mV start-up buck-boost DC/DC converter intended for multisource, low power systems. The LTC3106 powers low power wireless sensors from rechargeable or primary batteries supplemented by energy harvesting. The device incorporates maximum power point control (MPPC) making it compatible with common high impedance power sources, including photovoltaic cells, thermoelectric generators (TEGs) and fuel cells. LTC3106 operates over an input voltage range of 300 mV to 5.5V.



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BEWARE THIS INTEGRATION NIGHTMARE

BY JACOB BENINGO

Embedded software has come a long way in last 15 years let alone the last 40. While there are still many areas that developers and teams can improve in, firmware has for the most part moved away from single module monolithic programs with goto statements sprinkled everywhere. Code bases have become more organised and they are starting to take the shape of general purpose and object oriented software. Despite these advances, however, firmware integration may still be one of the biggest challenges facing software engineers today.

Most engineers attempt to reuse what has already been invented. If a library module exists, why rewrite it? Simply integrate it into the code base and have one less feature to worry about.

The problem is that the assumption many developers make - that libraries or open source code follow interface and software design similar to their own code - can be very far from the truth. Rather than speeding up development, then, integrating existing components could have the exact opposite effect and lengthen the development cycle instead.

Unfortunately, I recently encountered such a circumstance while developing a bootloader.

The ability to update a microcontroller's firmware in the field through a bootloader is a common and often critical feature of an embedded system. But it shouldn't be an entire development cycle unto itself. Over the past five years I have written dozens of bootloaders for nearly every microcontroller and interface imaginable. All of those development efforts have resulted in a modular bootloader framework with well-defined interfaces and documented pre- and post conditions. Writing a bootloader for a new device has become, for me, extremely fast and efficient -- exactly what a developer would want in a common system feature.

But not this time.

As with all development nightmares, it all started with a simple request: integrate the client's OS and use their serial driver and protocol to speed up development. Normally the code space of a bootloader should be minimised but in this case code size wasn't a primary factor. So, the request appeared to be no big deal. A quick examination of the serial driver gave the impression that it should be easy enough to integrate the driver into the existing bootloader framework.

Nothing could have been further from the truth.

The development effort started off being perfect. By leveraging existing templates and process, the effort jumped out ahead of schedule and was moving along at an amazing pace. Then we put the OS and serial driver into place and they seemed functional. The next step was to integrate the bootloader serial protocols with the existing serial driver. That is where the first integration issues arose.

The serial driver wasn't really a driver. Instead, it was a driver with a serial protocol already built into it. But the bootloader framework already used a (different) serial protocol. So, integrating the bootloader protocol into the customer's existing serial "driver" quickly became non-trivial.

In order to preserve the customer's existing protocol - because it was, of course, a "must have" - the serial driver now had to be modified. It needed to be able to decide whether the bootloader stream was being received or the original protocol was being received. This seems like a minor update and not a big deal, except that as it turned out the base OS code was meticulously balanced such that minor changes to the

code resulted in the system crashing. Before we could perform the integration of a simple serial protocol, an entire code base now had to be debugged to determine why seemingly minor changes caused the system to throw a major fit. This is not a trivial endeavour when the developer's knowledge about the code base is minimal - because the code was supposed to just work off-the-shelf.

Once we resolved the base code issues, we updated the serial "driver" to handle the bootloader protocol packets as well. One might think that the project would then move smoothly, but one would be mistaken. The well-tuned and oiled bootloader framework now required its own modifications to make its round construction fit into a square hole.

The integration of each bootloader feature ended up requiring a minor code change, but one that in turn resulted in an unexpected behaviour or bug that had to be carefully tracked and resolved. Eventually the two code bases were integrated, but it took nearly two weeks longer than originally anticipated and generated more issues than one might wish to recall.

On the surface, the use of an off-the-shelf or open-source code base can bring a developer the anticipation of a stress free and shorter development cycle. But beware. Embedded software development that uses outside contributions is riddled with assumptions based on incomplete information and unfounded expectations about the quality and design of the received software and hardware. The result is that while most such development efforts at first seem trivial, the devil and the delays will be found in the details.

Is using that open source library really saving you time and reducing cost?

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